Simulation and Experimental Validation of Multicarrier PWM Techniques for Three-phase Five-Level Cascaded H-bridge with FPGA Controller

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Abstract- The FPGA represents a valid solution for the design and implementation of control systems for inverters adopted in many fields of power electronics because of its high flexibility of use. This paper presents an overview and an experimental validation of the MC SPWM techniques for a three-phase, five-level, cascaded H-Bridge inverter with FPGA controller-based. Several control algorithms are here implemented by means of the VHDL programming language and the output voltage waveforms obtained from the main PWM techniques are compared in terms of THD%. Simulation and experimental results are analyzed, compared and discussed**.**

Keywords Multilevel Power Converter, PV systems, grid connected, FPGA, VHDL.

1. Introduction

Over the last decade the production of electrical energy has faced a significant increase, thanks to the Directive 2009/28/EC of the European Parliament and Council on the promotion of the use of energy from renewable sources with three main objectives: 20% of reduction of greenhouse gas emissions with respect to the levels detected in the year 1990, 20% of increase in terms of energy generated by renewable energy sources and 20% of energy saving within the year 2020. Indeed, by considering an economical viewpoint, both the feed-in-tariffs of many European countries and the reduction of the price for the components of photovoltaic systems have increased the number of PV sites. In addition, from a technological viewpoint, the adoption of new technologies for energy management, dynamic reconfigurations, PV cells and monitoring systems has increased the spread of the PV systems [1-7].

With respect to power converters they can be applied in many fields of application, such as electric drives [8-10] and renewable energies, bringing great advantages in terms of efficiency enhancement and energy savings. In particular Multilevel Power Inverters (MPI) represent a valuable choice for medium-voltage/ high-power applications with respect to converters of the traditional three-level type (power semiconductor switches present operative limits) [11] because of their lower harmonic content in terms of output voltage waveform. In addition, MPI can be suitably interfaced with renewable energy sources, according to [12].

By considering the previously described statements, this paper aims to present an experimental analysis of the main MC PWM modulation techniques for a three-phase, five level cascaded H-bridge inverter through means of a FPGA controller-based board, which represents a favorable solution for the design and implementation of control systems for inverters because of its high flexibility of use. The analysis is carried out in order to compare the proposed techniques and discuss about the most suitable solutions depending on the related converter application. For this purpose, the Total

Harmonic Distortion (THD%) and the DC link voltage Utilization (DCU%) are used as parameters of comparison.

More in detail, this paper is structured as follows: the multilevel power inverter structures and the multicarrier modulation techniques are described in Sections 2 and 3, respectively, whereas the Matlab/Simulink simulation results of the proposed techniques are summarized in Section 4. Finally, by means of a test bench specifically equipped for this purpose and with the implementation of the related software for the converter control (see Section 5), the experimental validation of these techniques on a Cascaded H-Bridge Multilevel Inverter prototype are proposed and discussed in Section 6.

2. Multilevel Power Inverter Structures

This Section reports the main MPI structures proposed in literature and their related advantages and drawbacks, according to [13,14].

Fig. 1 shows the three-phase, five-level structure of a DCMI (*Diode Clamped Multilevel Inverter*), which is composed by a DC-bus that charges an even number of capacitors with a central neutral point. The voltage V_{SI} applied to the switches during the interdiction phase for a converter with n_L levels is given by the following equation:

$$V_{SI} = \frac{V_{DC}}{n_L - 1} \quad (1)$$

Fig. 2 shows the scheme referred to the CCMI (*Capacitor Clamped Multielvel Inverter*) structure, which is composed by a DC-bus, split through a set of capacitors with a central neutral point. The output voltages are given by the composition between the DC-bus voltage and the clamp diode voltage. By choosing appropriate combinations, several intermediate voltage levels can be obtained. In addition, the active power (as well as the reactive power) can be controlled in a simpler manner if compared with other topologies of multilevel converters.

Finally, the structure of a CHBMI (*Cascaded H-Bridge Multilevel Inverter)* is composed by several H-bridges, as shown in Fig. 3.

The output converter voltage (e.g. for phase *a*) is given by the sum of the voltages generated by the n series-connected modules of each phase:

$$V_a = \sum_{i=1}^{n} V_{AN,i} \quad (2)$$

The number of levels n_L can be expressed as a function of the number of the H-bridges, here named n_{HB}:

$$n_L = 2n_{HB} + 1 \quad (3)$$

In addition, the latest topology is intrinsically fault tolerant, even though its application is limited due to the need of separate DC sources.

Table 1 summarizes the main advantages and drawbacks of the proposed topologies. Among the previously described structures, the CHBMI topology can be considered the most suitable choice in the field of PV systems, due to both its modular structure (allowing a simpler add of more levels) and to the lower number of components needed for its realization. However, each structure can be suitable for specific applications [14,15].

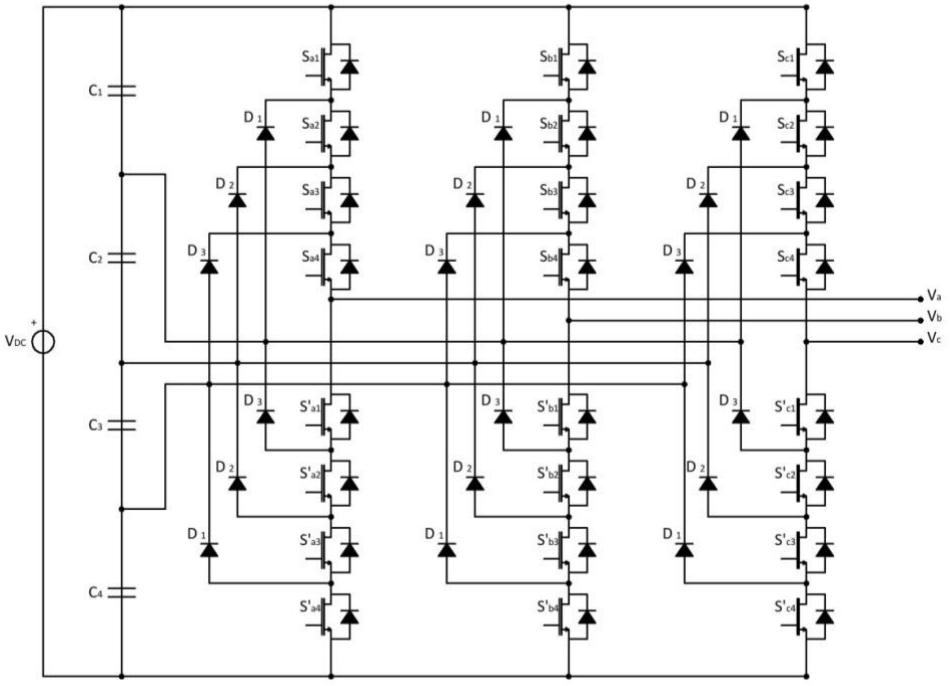


Fig. 1. Three-phase five-level structure of a DCMI.

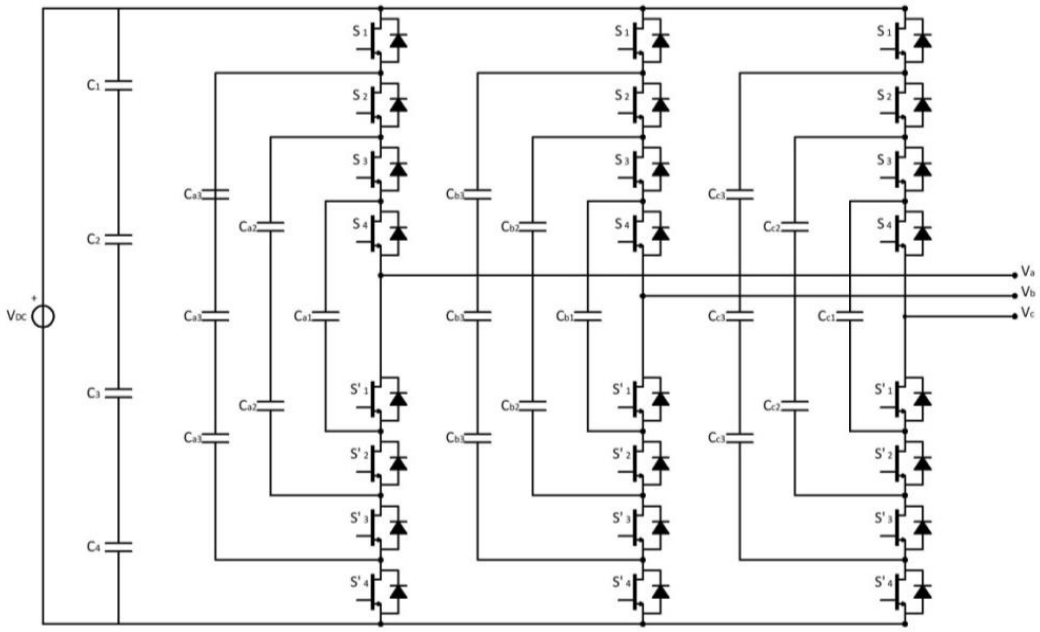


Fig. 2. Three-phase five-level structure of a CCMI.

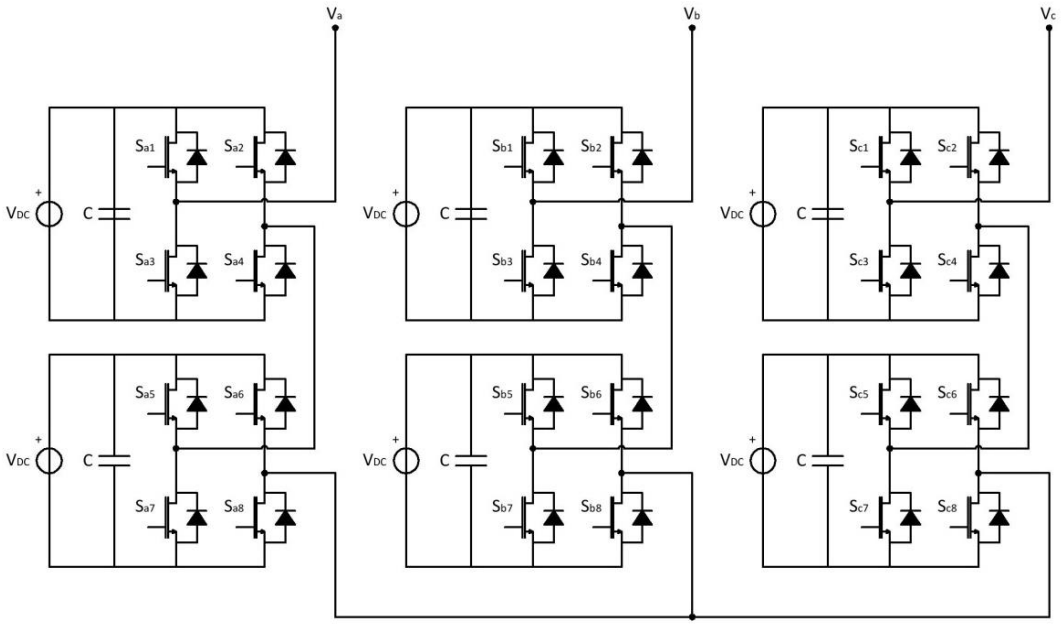


Fig. 3. Three-phase five-level structure of a CHBMI.

Table 1. Advantages and drawbacks of the Multilevel Power Inverters

Converter type	Advantages	Drawbacks
DCMI	High efficiency	Complexity of the control system High number of clamp diodes
CCMI	Simpler control of active and reactive power	Unbalance of capacitor voltages High number of capacitors High costs
CHBMI	Fault tolerant	Requirement of separate DC sources

3. Overview of Multicarrier Modulation Techniques

The Pulse Width Modulation (PWM) techniques usually adopted for converters of the traditional type can be also applied to multilevel converters. In this case, the techniques are named MC PWM (Multicarrier Pulse Width Modulation) [16-18]. The most popular modulation techniques for MPI use several triangle carrier signals and one modulating signal per phase. By considering the CHBMI structure, the command signals delivered to the components of the same leg of the bridge are obtained through the comparison between each carrier signal and the modulating signal.

For a MPI with a number of levels equal to n_L, the number of carrier signals N_c is given by the following equation:

$$N_c = n_L - 1 \tag{4}$$

The modulation index m can be expressed as function of n_L:

$$m = \frac{A_M}{A_C(n_L - 1)} \tag{5}$$

A_M is the amplitude of the modulating signal, whereas A_C is the amplitude of the carrier signal.

Moreover, the index of frequency modulation m_f is given by the ratio between the frequency of the carrier signal f_C and the frequency of the output fundamental signal f_1:

$$m_f = \frac{f_C}{f_1} \tag{6}$$

In literature, several MC PWM modulation techniques for multilevel inverters are provided. In particular, depending on the phase shift among the carrier signals, the following dispositions can be obtained:

- Phase Disposition PWM (PD PWM);
- Phase Opposition Disposition PWM (POD PWM);
- Alternative Phase Opposition Disposition PWM (APOD PWM);
- Phase Shifted (PS PWM);

Depending on the modulating signal waveform, the following techniques can be obtained:

- Sinusoidal PWM (S PWM);
- Third Harmonic Injection (THI PWM);
- Switching Frequency Optimal (SFO PWM);

The THI PWM modulating signal consists in a sinusoidal reference signal with an injection of a third harmonic signal, whose magnitude is equal to the 25% of the fundamental. The SFO PWM modulating signal can be obtained by subtracting to a sinusoidal reference signal the voltage-offset v_{offset}, which is defined as follows:

$$v_{offset} = \frac{\max(v_a, v_b, v_c) + \min(v_a, v_b, v_c)}{2} \tag{7}$$

where v_a, v_b and v_c are the instantaneous values of the reference voltage.

Therefore, the instantaneous values of the modulating signals are given by:

$$v_{a,SFO} = v_a - v_{offset} \tag{8}$$

$$v_{b,SFO} = v_b - v_{offset} \tag{9}$$

$$v_{c,SFO} = v_c - v_{offset} \tag{10}$$

The sinusoidal modulating signal is a very popular method, commonly adopted in commercial inverters for industrial applications, whereas the THI PWM and SFO PWM techniques allow a better DC link voltage utilization at high modulation indices.

From the combination between the carrier signals and the modulating signals, twelve modulation techniques are obtained and graphically summarized in Fig. 4 (a-n) [17-19].

4. Simulation Results Analysis and Discussion

This Section describes the implementation in the Simulink® environment of the modulation techniques described in Section 3, with the purpose of evaluating the harmonic content of both the output phase and line voltages of the proposed converter. This analysis is achieved by means of the Total Harmonic Distortion (THD%), which can be evaluated as follows [20-21]:

$$THD\% = \sqrt{\frac{V_{rms}^2 - V_{rms,1}^2}{V_{rms,1}^2}} \cdot 100 \tag{11}$$

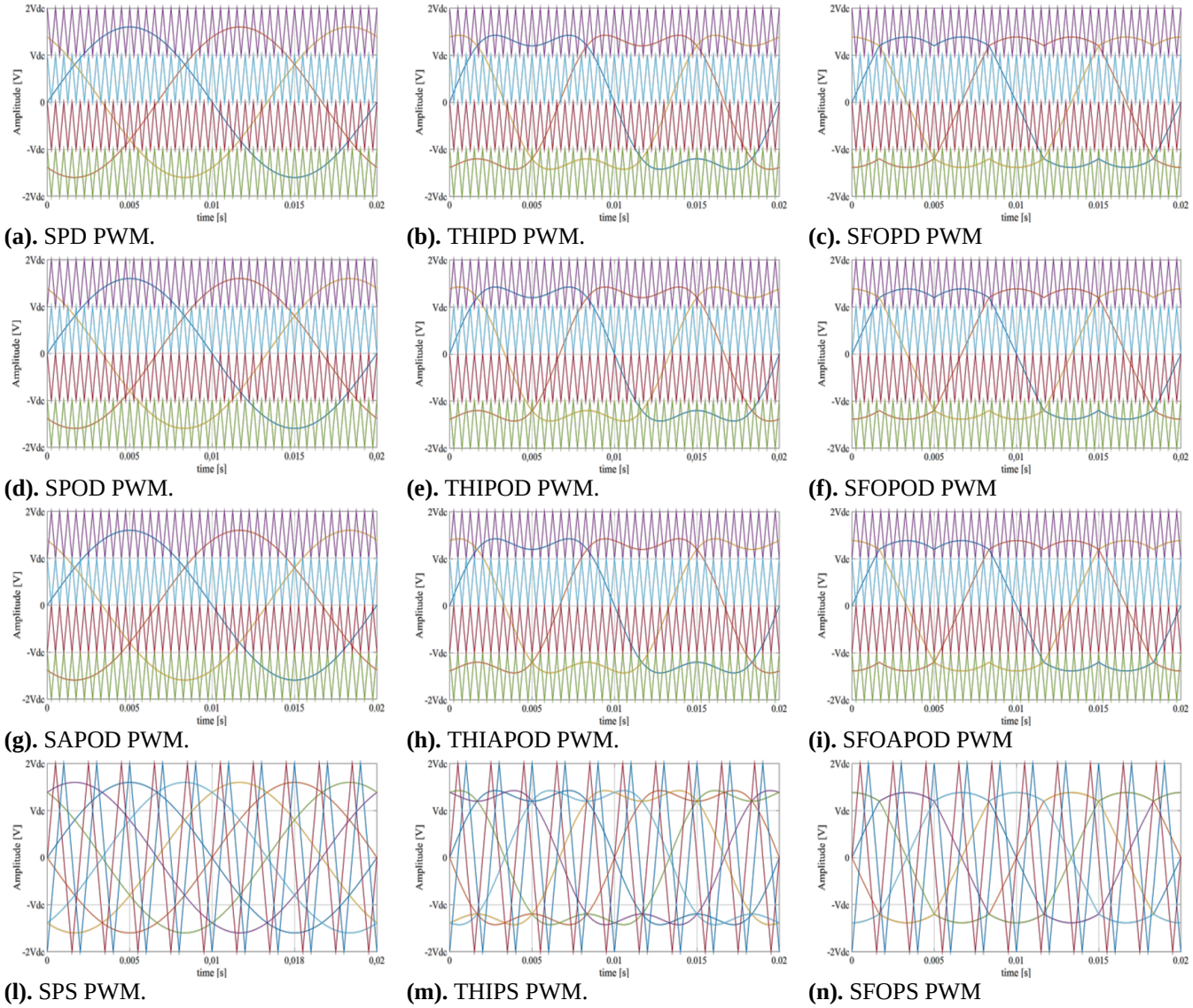
where V_{rms} is the root mean square value of the phase voltage and $V_{rms,1}$ is the rms value of its fundamental harmonic.

Moreover, in order to compare the performances of the converter with the proposed modulation techniques, the parameter named DC link voltage Utilization (DCU%) has been taken into account. This parameter is defined as the ratio between the output fundamental voltage and the DC link voltage:

$$DCU\% = \frac{V_{rms,1}}{V_{dc}} \cdot 100 \tag{12}$$

where V_{dc} is the amplitude of the DC link voltage.

A three-phase, five-level converter with CHBMI circuital structure has been simulated for the proposed analysis. The simulation has been carried out by changing the modulation index *m* from 0.2 to 1.4 and by choosing the switching frequency equal to 10 kHz. In this way, it is possible to evaluate the converter performances both in the field of linear modulation and in overmodulation. Therefore, for each of the proposed carrier signals, the THD% and the DCU% have been computed for the three considered modulating signals and by varying the modulation index. The THD% trends of the line voltage (a) and the phase voltage (b) obtained with the Sinusoidal (blue color), THI (red color) and SFO (yellow) for each of the proposed carrier signals are all reported in Figs. 5-8.



(a). SPD PWM. **(b).** THIPD PWM. **(c).** SFOPD PWM

(d). SPOD PWM. **(e).** THIPOD PWM. **(f).** SFOPOD PWM

(g). SAPOD PWM. **(h).** THIAPOD PWM. **(i).** SFOAPOD PWM

(l). SPS PWM. **(m).** THIPS PWM. **(n).** SFOPS PWM

Fig. 4 (a-n). Graphical overview of the proposed modulation techniques.

From the analysis of Fig. 5 (a) it can be noticed that the THD% values are almost comparable for each technique and through all the modulation range. In addition, according to Fig. 5 (b), for m>0.5 the related THD% is lower than 50%, due to the fact that the voltage waveform turns into five levels. Furthermore, for modulation indexes higher than 0.7, the THD% values of the SPD are considerably lower than those obtained with the other techniques. From Fig. 6 it appears clear that the THD% values obtained with the proposed techniques are comparable only for modulation indexes lower than 0.5, while for *m* ranging between 0.5 and 0.8 the lowest THD values are obtained with the THIPOD and the SFOPOD techniques. The phase voltage THD% obtained from the SPOD, THIPOD and SFOPOD techniques are similar to those of Fig. 5. As well as for the previous cases, the THD% trends obtained for the SAPOD, THIAPOD and SFOAPOD techniques (see Fig. 7) are almost comparable with those of Figs. 5 and 6. Other interesting results are plotted in Fig. 8, which shows the THD% results for the SPS, THIPS and SFOPS techniques. The SPS guarantees lower THD% values of the line voltage if *m* is confined within the area of linear modulation. Besides this region, the three trends are almost comparable, as well as for the phase voltage trend. In any case, the lowest possible THD% value is obtained for m=0.6 and adopting the SFO as modulating signal. From the previously reported graphs, it can be stated that the lowest average THD values are obtained for a sinusoidal modulating signal. Fig. 9 reports the comparison between the THD% trends as function of *m* for techniques with a sinusoidal modulating signal and with all the proposed carrier signals (PD in blue color, POD in red color, APOD in yellow color and PS in magenta color). It can be observed that the lowest THD% values in the region of linear modulation are obtained for the SPD technique, whereas these values are comparable in the overmodulation region. Furthermore, the SPS technique is suitable in terms of the phase voltage. The comparisons between the DCU% of each of the proposed techniques are all reported in Fig. 10 (a-d), from which it can be stated that the DC utilization is lmost the same in the linear region, while the THI and SFO techniques are better suited in the overmodulation area

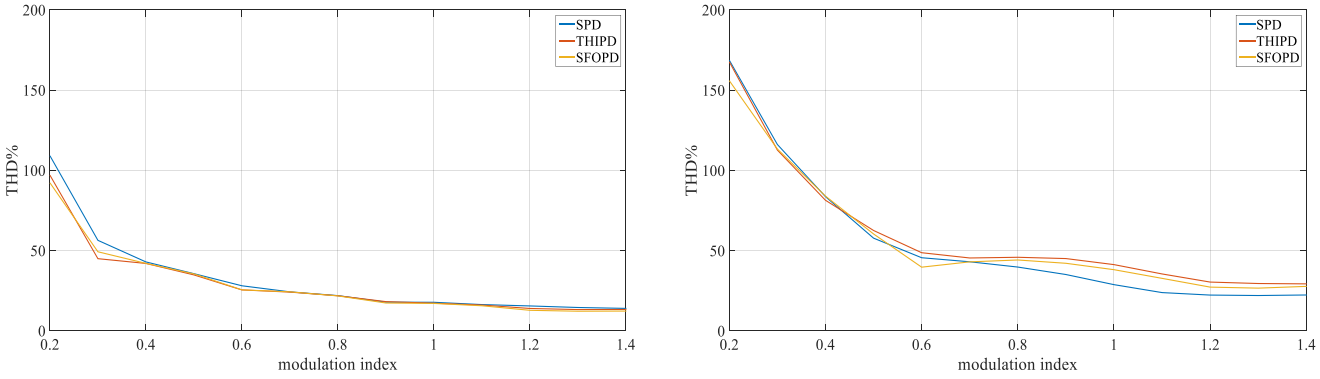


Fig. 5. THD% comparison as function of the modulation index for SPD, THIPD and SFOPD: (a) line and (b) phase voltage.

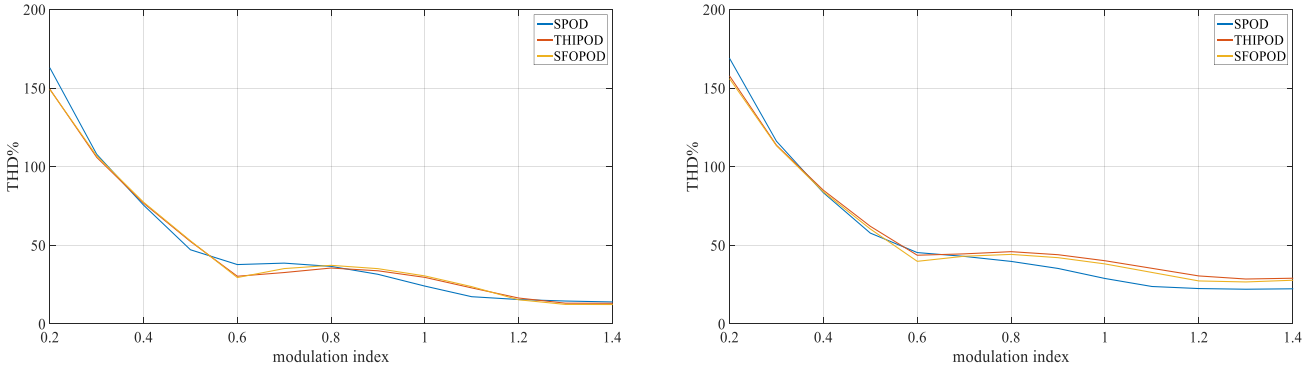


Fig. 6. THD% comparison as function of the modulation index for SPOD, THIPOD and SFOPOD: (a) line and (b) phase voltage

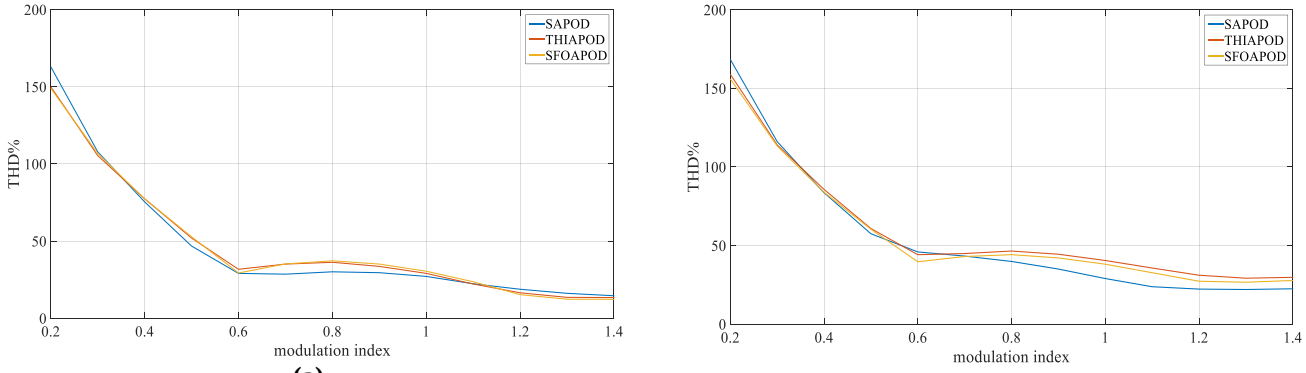


Fig. 7. THD% comparison as function of the modulation index for SAPOD, THIAPOD and SFOAPOD: (a) line and (b) phase voltage

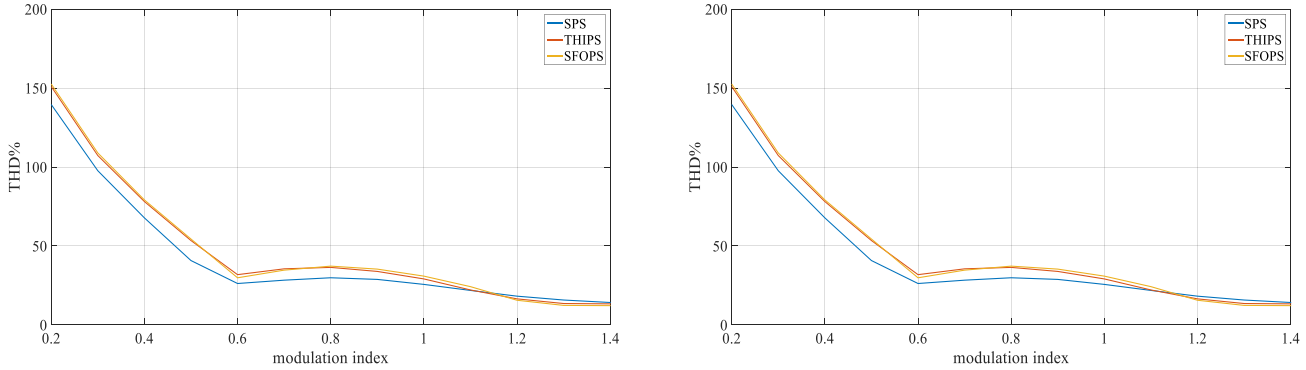
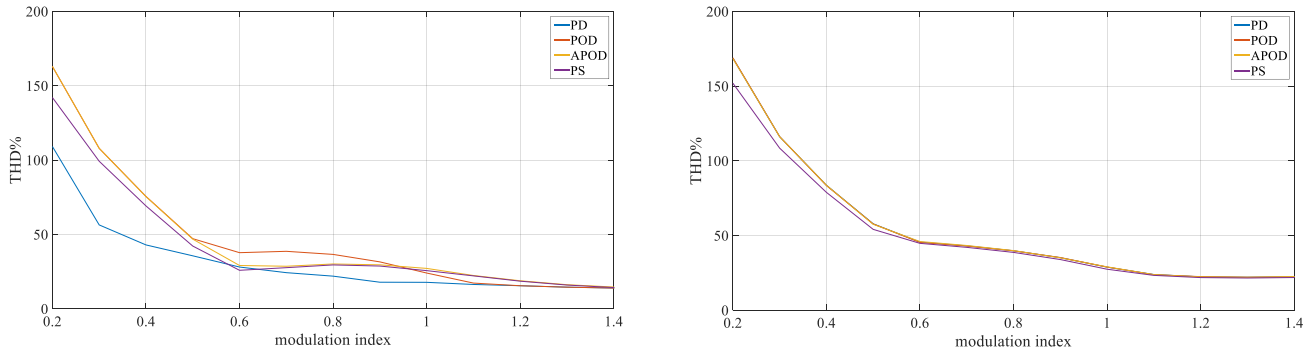
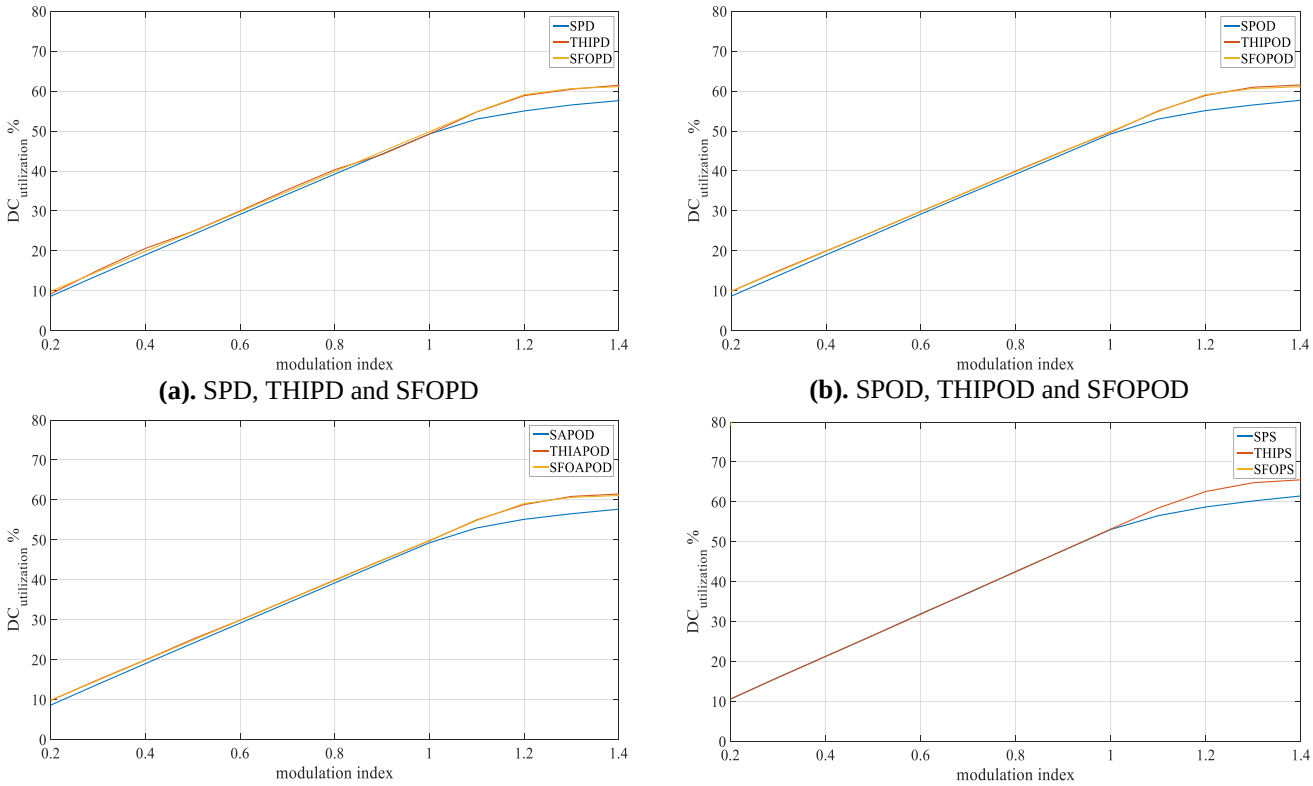


Fig. 8. THD% comparison as function of the modulation index for SPS, THIPS and SFOPS: (a) line and (b) phase voltage



(a). **(b)**

Fig. 9. THD% comparison as function of the modulation index for SPS, SPOD and SAPOD: (a) line and (b) phase voltage



(a). SPD, THIPD and SFOPD

(b). SPOD, THIPOD and SFOPOD

(c). SAPOD, THIAPOD and SFOAPOD

(d). SPS, THIPS and SFOPS

Fig. 10. THD% comparison as function of the modulation index for SPS, SPOD and SAPOD: (a) line and (b) phase voltage

5. Design and Implementation of the Software for the Converter Control

In order to control the amplitude and frequency of the fundamental output voltage of the inverter, all the techniques described in Section 3 have been implemented by means of an FPGA Altera Cyclone III EP3C40Q control board [22-24], providing faster I/O time responses, rapid prototyping and an online reconfiguration, eliminating the relatively high costs for redesign and maintenance. The block scheme of the control, which has been obtained with the Quartus II software, is shown in Fig. 11 [25,26]. The latter has been implemented by using the VHDL programming language [27]. The block scheme of the control software, particularized for the SAPOD technique, implemented in the Quartus II environment is shown in Fig. 11. From a 100 MHz clock signal, by means of a digital PLL circuit, the clock signals both for the modulating and the carrier signals are obtained, equal to 10 kHz and 5 MHz, respectively. The modulating signals have been all implemented in one block named "sintrifasefive" and discretized with 200 samples in a period. Each of the output modulating signals are, then, sent and compared to the triangular carrier signals, generating the gate signals for the related control of the components. More in detail, for each comparison the gate signal is set to 1 if the modulating signal is higher than the carrier one, otherwise it is set to 0. Therefore, for a complete analysis, twelve control software have been implemented in the QUARTUS II environment. Fig. 12 shows the waveforms carried out from the simulation of the proposed control.

6. Experimental Results Analysis and Discussions

In order to carry out the experimental analysis, a three-phase, 5 level DC/AC converter prototype with a CHBMI

circuital structure has been assembled. The test bench is shown in Fig. 13 and it is mainly composed by:

- A prototype of FPGA-based control board (Cyclone III – ALTERA, DigiPower s.r.l);
- Six prototypes of power MOSFET-based H-bridges (DigiPower s.r.l, model IRFB4115PbF), whose technical features are summarized in Table 2 [28];
- A Teledyne LeCroy WaveRunner 6Zi, scope, used for the real-time monitoring and acquisition of the related waveforms;
- Six DC sources with 12V of rated voltage;
- A balanced RL three-phase electric load.

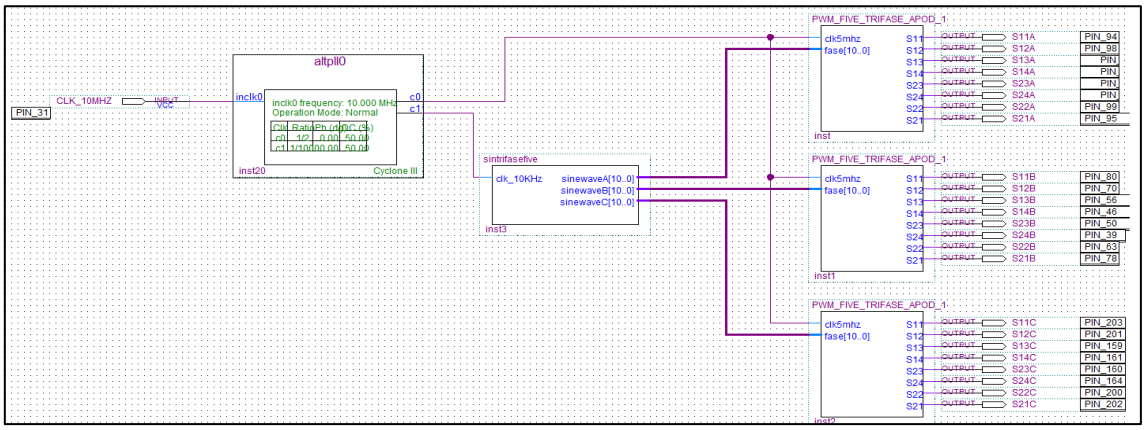


Fig. 11. Block scheme of the control software.

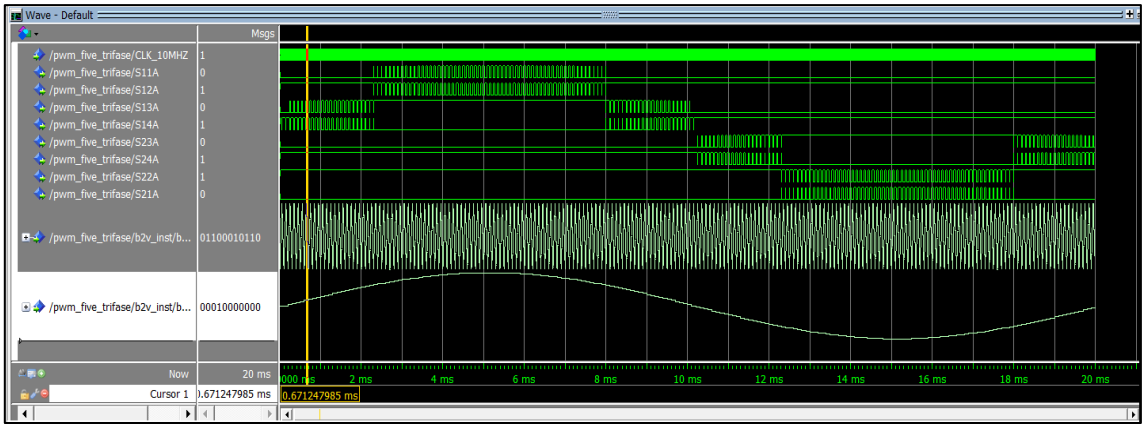


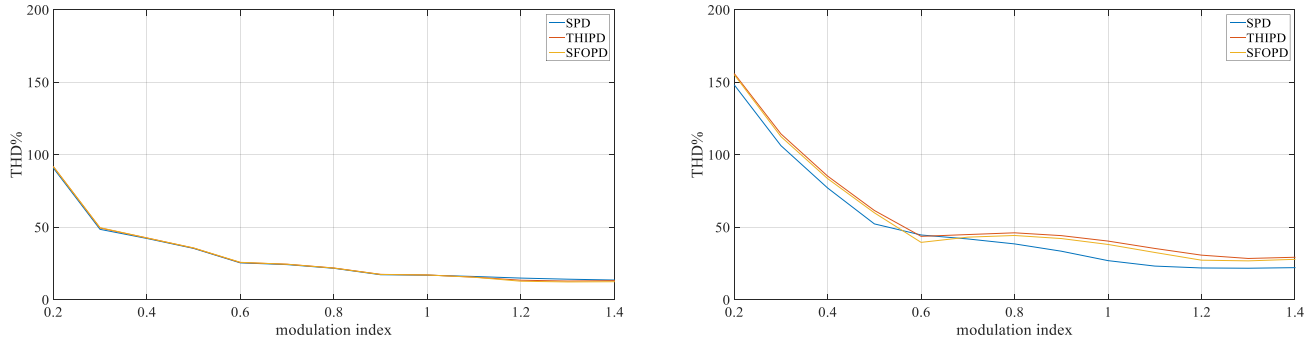
Fig. 12. ModelSim results

Fig. 13. A photograph of the test bench.

Table 2. Technical features of the IRFB4115PBF device

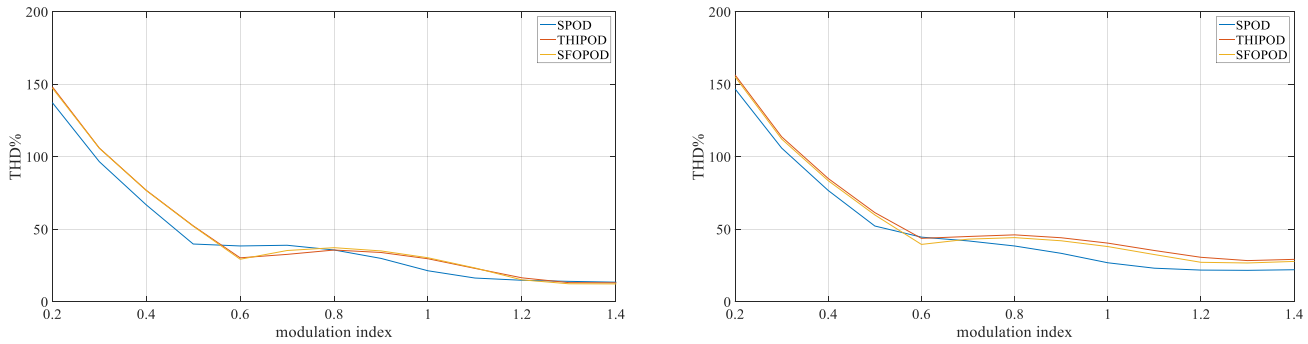
Quantity	Symbol	Value
Voltage	V_{dss}	150 V
Resistance	$Rds_{(on)}$	9.3 mΩ
Current	$I_{d\ (silicon\ limited)}$	104 A
Turn on delay	$T_{D(ON)}$	18 ns
Rise time	t_R	73 ns
Turn off delay	$T_{D(OFF)}$,	41 ns
Fall time	t_F	39 ns
Reversal recovery	t_{RR}	86 ns

By means of the described test bench, the proposed techniques have been experimentally implemented. The voltage waveforms have been acquired by the Teledyne LeCroy WaveRunner 6Zi acquisition system with a number of samples equal to 1 Ms and in a time interval equal to 20 ms, corresponding to a sampling frequency of 50 MHz, for modulation techniques with PD, POD and APOD based. For the PS modulation techniques, 5 Ms of samples have been acquired, corresponding to a sampling frequency of 250 MHz (the PS allows the obtainment of a spectrum shifted four times with respect to the switching frequency). Figs 14-17 show the THD% values experimentally determined as function of *m* for each of the proposed technique. As previously discussed in Section IV, the adoption of a PD carrier signal allows the obtainment of similar results in terms of THD% for the line voltages, while the lowest THD values for phase voltages are obtained with a sinusoidal modulating signal for all the range of the modulation index (see Fig.14). As expected, similar results are obtained also for the THD% values experimentally carried out with POD, APOD and PS carrier signals (see Figs. 15-17, respectively), if compared with the simulated THD values (see Section IV, Figs. 6-8). The adoption of a sinusoidal modulating signal allows the obtainment of the lowest THD% values for all the range of *m* and for both phase and line voltages. The THD% trends as function of *m* obtained with a sinusoidal modulating signal for each of the proposed carrier signals are all plotted in Fig. 18, from which it appears evident that the lowest THD% values for the line voltage are obtained through means of the SPD modulation technique (Fig. 18a). The THD% values for the phase voltage are almost comparable, as shown in Fig. 18 (b), which is in accordance with the simulated results discussed in Section IV. Moreover, Fig.19 shows the DCU% trends experimentally obtained for all the proposed modulation techniques. As well as for the previous case, the experimental results are comparable with the simulated ones (see Section 4). Finally, Fig. 20 (a-b) shows some examples of THD% obtained for both the line and phase voltages experimentally detected by adopting the modulation techniques previously discussed in this paper with *m*=0.8.



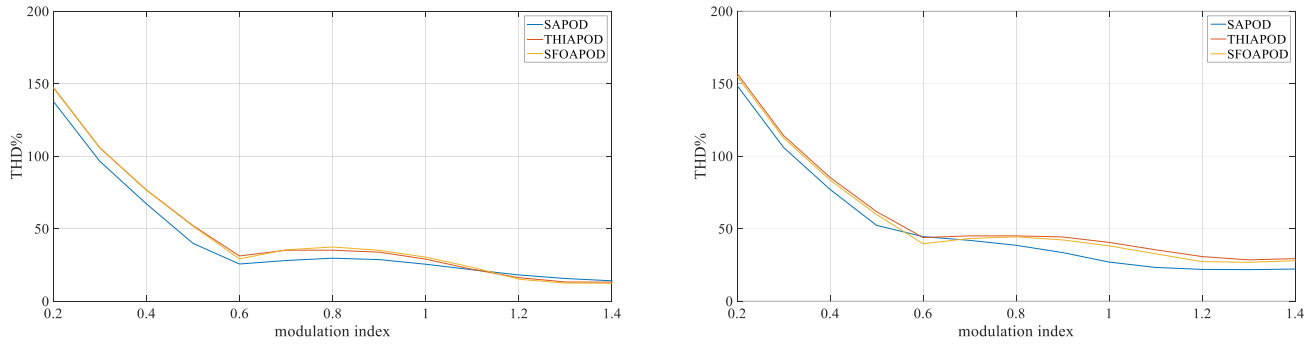
(a). **(b)**

Fig. 14. Experimental results of the THD% for (a) line voltage and (b) phase voltage: SPD, THIPD and SFOPD techniques.



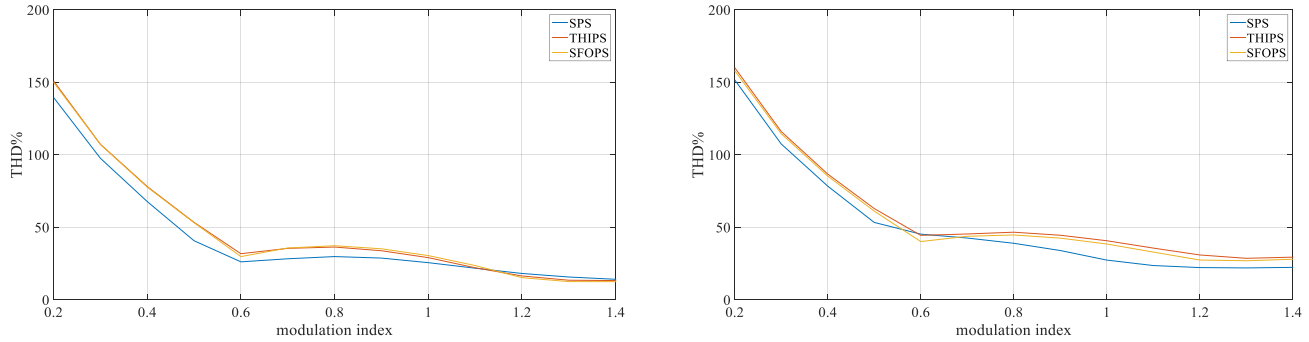
(a). **(b)**

Fig. 15. Experimental results of the THD% for (a) line voltage and (b) phase voltage: SPOD, THIPOD and SFOPOD techniques.



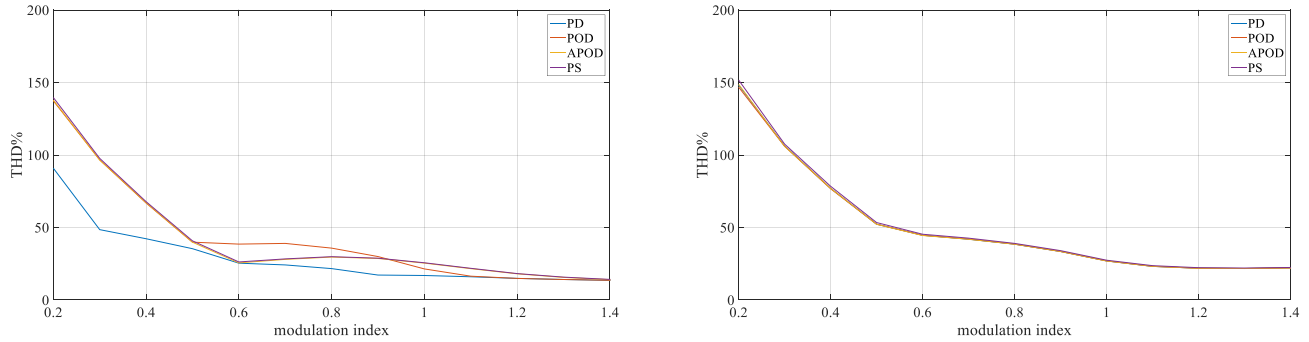
(a). **(b)**

Fig. 16. Experimental results of the THD% for (a) line voltage and (b) phase voltage: SAPOD, THIAPOD and SFOPAOD techniques.



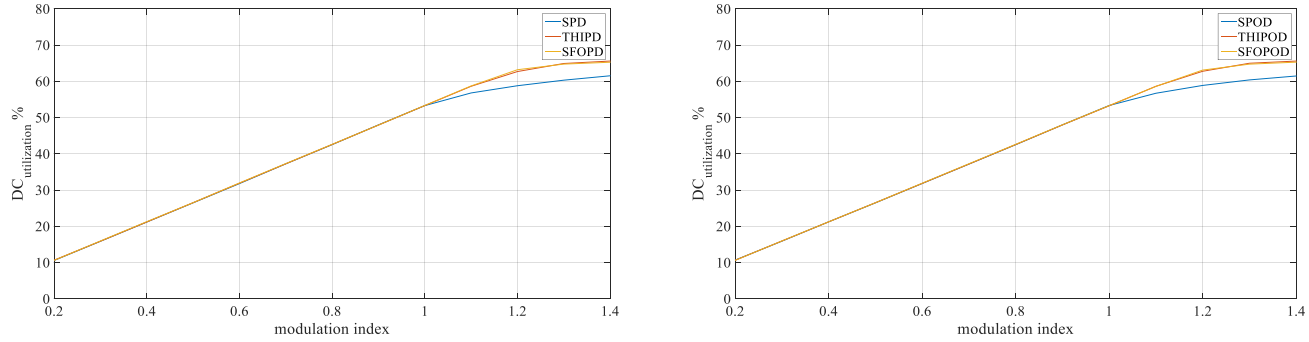
(a). **(b)**

Fig. 17. Experimental results of the THD% for (a) line voltage and (b) phase voltage: SPS, THIPS and SFOPS techniques.

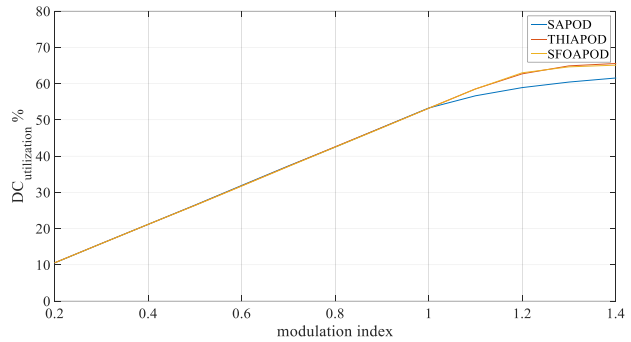


(a). **(b)**

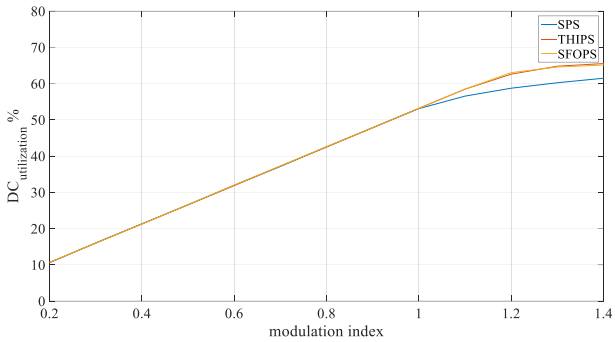
Fig. 18. Experimental results of the THD% for (a) line voltage and (b) phase voltage: SPD, SPOD, SAPOD and SPS techniques.



(a). SPD, THIPD and SFOPD **(b).** SPOD, THIPOD and SFOPOD

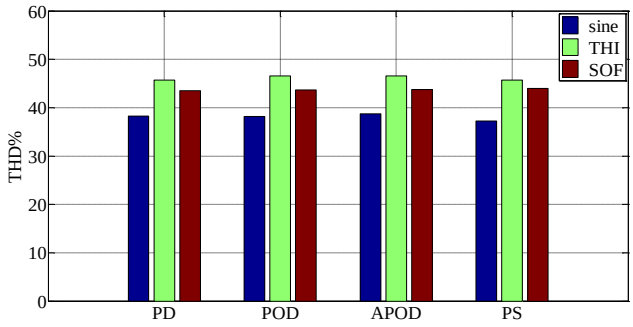


(c). SPD, THIPD and SFOPD

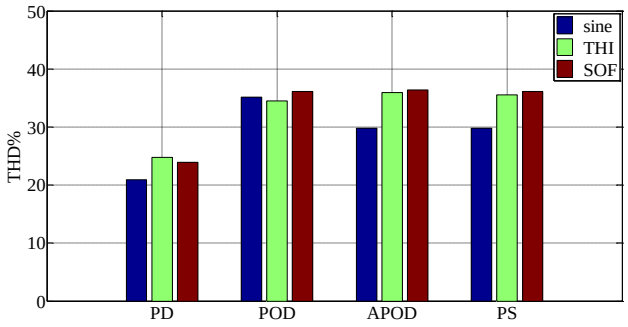


(d). SPOD, THIPOD and SFOPOD

Fig. 19. Experimental results of the DCU% as function of *m*.



(a)



(b)

Fig. 20. THD% of phase voltage (a) and line to line voltage (b) with *m* = 0.8.

7. Conclusion

This paper has presented the simulation and experimental analysis of the MC PWM techniques for five level, three-phase, cascaded H-bridge inverter with FPGA controller-based through the VHDL control software. The comparison between the proposed modulation techniques has been performed by means of the THD% and the DCU%. The simulations and experimental results are almost comparable for each of the proposed technique. With regards to the phase voltage, by adopting the sinusoidal modulating signal, the minimum value of the THD% is achieved. Moreover, by comparing the proposed carrier signals with the same sinusoidal modulating signal, it can be stated that the SPD represents the most suitable solution in terms of minimum THD% value, for the line voltage. On the contrary, for the phase voltage, the best choice is strictly related to the specified application, because the THD% values are almost variable in dependence of the modulation index. Finally, in terms DCU%, it can be noticed that the differences between the proposed techniques are not as significant as expected in the linear modulation region, whereas for the overmodulation region the THI and the SFO modulating signals allow the obtainment of the optimum DCU% value.

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