Simulation and Performance Study of Nanowire CdS/CdTe Solar Cell

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Abstract - Thin film CdS/CdTe solar cell is one of the leading technologies for providing high power conversion efficiency at comparatively low manufacturing cost. We have done modeling and simulation of thin film CdS/CdTe solar cell and then used nanowire CdS layer instead of planar CdS layer using SCAPS-1D to demonstrate the fact that the use of CdS nanowires enhances the efficiency of the CdS/CdTe solar cells by ~3%. The scattering cross section of CdS nanowire was observed using Lumerical FDTD solutions to determine that diameter of 40-60nm is preferable for CdS nanowires for using as window layer of CdS/CdTe solar cell. For thin film CdS/CdTe solar cell the open circuit voltage was 0.69V and efficiency was 15.42%. For nanowire CdS/CdTe solar cell model the open circuit voltage was 0.82V and efficiency was 18.30%. Device parameters such as: temperature, interface state density, density of states, electron and hole mobility and metal work function were studied which can affect the efficiency of the nanowire CdS/CdTe solar cell. The rollover effect on nanowire CdS/CdTe solar cell was explained by varying the majority carrier barrier height of back contact from 0.4 to 0.7 eV. This indicates that when the barrier height is increased, a roll over effect occurs and the efficiency decreases. Effects of the parameters mentioned above were observed in order to ensure high efficiency performance from nanowire CdS/CdTe solar cell.

Keywords - Cadmium Sulfide, Cadmium Telluride, Solar Cells, SCAPS-1D, FDTD Solutions, Interface State, Thin Film Solar Cell, Nanowire.

1. Introduction

Thin film CdS/CdTe solar cell draws attention for having p-type CdTe absorber layer along with n-type CdS as window layer, leading to low manufacturing cost and high optoelectronic efficiency. CdTe has a direct bandgap of 1.45 eV. CdTe is preferred as absorber layer for its high absorption coefficient (> 5 × 10^5 cm^{-1}). CdS is also a direct bandgap material and has a band gap of 2.4 eV. The difference of their bandgap makes CdS suitable as window layer of CdS/ CdTe Solar Cell. Also, the bandgap of CdTe is almost ideal for solar cells. Thus, compared to other materials, a thin layer of CdTe can act as absorbing layer. Due to this, the manufacturing cost of CdTe solar cell is quite low. Recent studies show that CdS/CdTe solar cell exhibited a nearly ideal spectral response of quantum efficiency and have strong reliability [1]. Most of the fabrication process of Thin film CdS/CdTe solar cell has some shortcomings. The main drawbacks are: short circuit of Transparent Conductive Oxide(TCO) layer and the CdTe layer when CdS layer is very thin and trap density inside the CdTe layer which is responsible for short minority carrier life time [2]. To get rid of these flaws, nanostructured geometries are introduced.

Goals of applying nanostructures in solar cells are to lower the manufacturing cost and to obtain higher power conversion efficiency. Comparing with traditional planar solar cells, much less materials are used in nanostructured solar cells and which makes them relatively inexpensive.

The structure of nw(nanowire) CdS exhibits advantageous optical properties due to its large surface area, high aspect ratio (depending on their length and diameter) and direct light absorption [3]. Moreover, CdS nanowires performs better than CdS thin-films as window layer of solar cells in photo-conversion process. Reduced reflection, extreme light trapping, strain relaxation, improved band gap tuning and increased defect tolerance are observed when CdS nanowires are involved in window layer of CdS/CdTe solar cell [4].

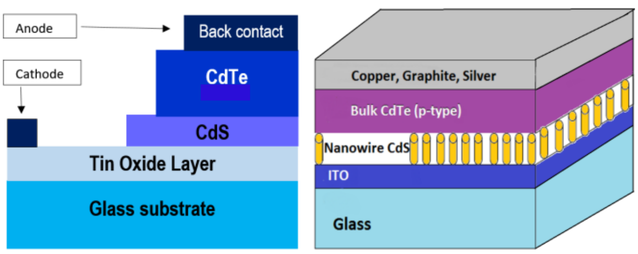
It is proven that the nw CdS layer has higher transmittivity than the thin film CdS window layer. The EDRL researchers observed that the absorption peak of CdS nanowires is slightly shifted towards the blue region of the sun light, from 512 nm for thin film film CdS solar cells to 480 nm for nanowire CdS solar cells. Thus, more photons were absorbed by CdTe layer which increased the light generated current [5].

The effective energy bandgap of nanowire CdS is higher than planar CdS film. Quantum confinement effects can be achieved by using CdS nanowires as window layer in CdS/CdTe solar cell, which ensures better performance as a semiconducting device. Due to higher energy band gap, reduced absorption in the ultra-violet portion of the solar spectrum and increased transmission of sunlight was noticeable for 300-600nm wavelength for nanowire CdS window layer. [6].

2. Modeling and Simulation

In this work, modelling and simulation for thin film CdS/CdTe solar cell and nanowire CdS/CdTe solar cell were done using a one dimensional solar cell simulation software SCAPS-1D. The scattering cross section for parallel and perpendicularly polarized excitation were obtained from Finite Difference Time Domain (FDTD) simulations to select proper diameter of CdS nanowire for nanowire CdS/CdTe solar cell. We have modeled our nw CdS/CdTe solar cell by following the design developed by Hongmei Dang et. al [7], where the fabrication of CdS nanowires was done by electrodeposition method and the CdTe absorber layer was fabricated by close-space-sublimation method. For modelling, thin film CdS/CdTe solar cell, we have considered fabrication process used by Jianhao Chen et. al. [7], where the synthesis of CdTe layer was done using Close-Space Sublimation (CSS) and CdS layer was formed using Chemical Bath Deposition (CBD) technology.

Figure 1(a) shows the schematic diagram of CdS/CdTe solar cell with planar thin film CdS structure whereas figure 1(b) shows same structure with CdS layer as nanowire CdS structure.



(a) (b)

Fig.1. (a) Thin film CdS/CdTe solar cell (b) Nanowire CdS/CdTe solar cell

In this work, the effect of light wavelength and scattering cross section have been observed for nanowires of diameter 10nm-100nm using FDTD calculations.

In figure 2, the graph shows that from wavelength of 400nm to 600nm, as diameter increases, scattering increases at a high rate. Besides, scattering decreases with the increase of wavelength. For using a nanowire for solar cell, it must be able to absorb light as much as it can and scattering of light should be minimum. These indicates that large diameters should be avoided. The graph depicts that, diameter of nanowires should be within 10-60nm because above this range, the nanowire will be more susceptible of scattering loss. Generally, nanowires of 40-60nm diameter with the length of 100nm are used for solar cell fabrication [6], [8]. In Fig. 2, scattering is negligible for 40nm. So, our simulated result is in accord with the experimental findings.

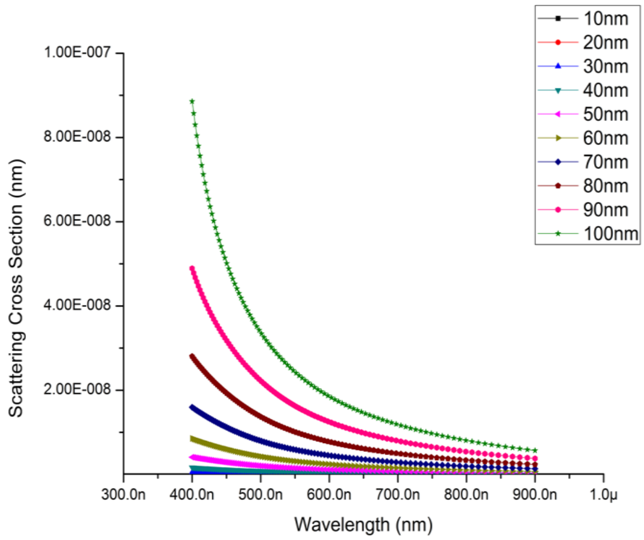


Fig. 2. Variation of scattering cross section with the change of diameter of CdS nanowire

3. Comparison between Nanowire CdS/CdTe SC and Thin Film CdS/CdTe SC

SCAPS-1D simulations has been done for both of the structures shown in figure 1(a) and 1(b) to understand the effect of using nanowire CdS instead of thin film CdS as window layer. Figure 3(a) and 3(b) shows the I-V characteristics of thin film CdS/CdTe and nw CdS/CdTe solar cell. Though short circuit current does not change noticeably, the open circuit voltage increases for nw CdS/CdTe solar cell due to reduced junction area resulting lower reverse saturation current. The efficiency has also been increased from 15.42% to 18.30% as summarized in Table 3.

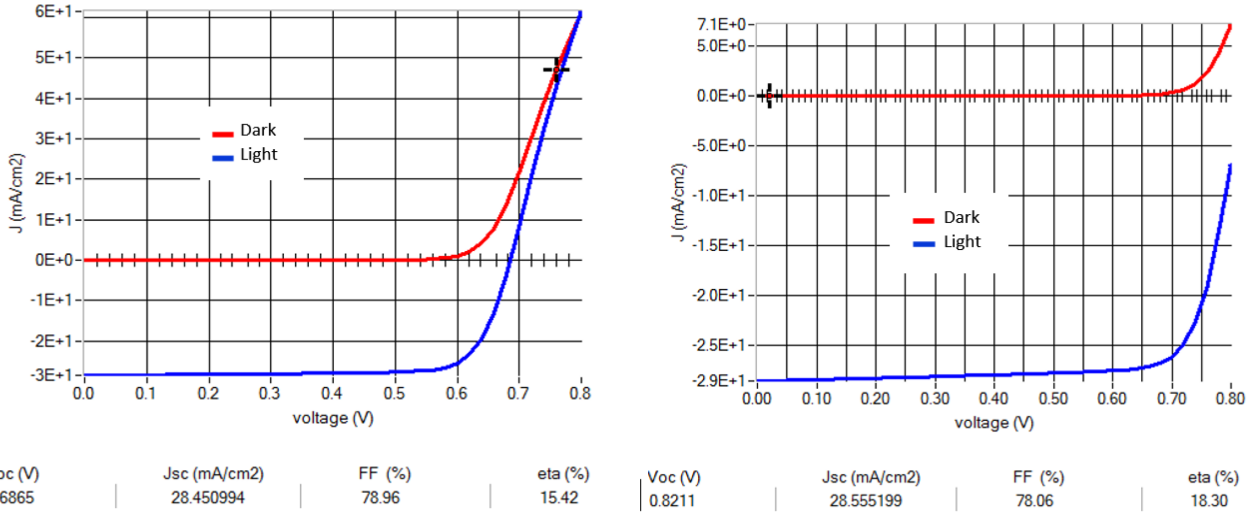
The parameters used in Table 1 and Table 2 for the simulation of thin film CdS/CdTe solar cell and nw-CdS/CdTe solar cell are all based on experimental study, literature values or in some cases reasonable estimation in accord with the simulation procedure [6], [8], [9], [10]. Defects were considered for CdTe, Planar CdS, NW CdS, CdS-nw/CdTe interface and i-SnO_2 layer considering the density of states.

Table 1. Parameters used for simulation of thin film CdS/CdTe solar cell and nw CdS/CdTe solar cell using SCAPS-1D

Parameters	**CdTe**	**Planar CdS** (For thin film CdS/CdTe SC)	**NW CdS** (For nw CdS/CdTe SC)	**CdS-nw/CdTe interface**	**i-SnO_2**	**ITO**
thickness (μm)	10	0.10	0.10		0.15	0.16
bandgap (eV)	1.5	2.42	3.50		3.6	3.7
electron affinity (eV)	3.93	4.20	4.0		4.4	4.8
dielectric permittivity (relative)	9.5	8.9	9.0		9.0	8.9
CB effective density of states (1/cm3)	1E+17	1.5E+18	9E+19		2.2E+19	5.2E+18
VB effective density of states ($1/cm^3$)	9E+18	1.8E+19	9E+18		2E+19	1E+18
electron thermal velocity (cm/s)	1E+7	1E+7	1E+7		1E+7	3E+7
hole thermal velocity (cm/s)	1E+7	1E+7	1E+7		1E+7	1E+7
electron mobility (cm^2/Vs)	3.2E+2	1E+2	1.2E+2		1.2E+2	2E+1
hole mobility (cm^2/Vs)	4E+1	2.5E+1	3E+1		3E+1	2E+1
shallow uniform acceptor density N_A ($1/cm^3$)	1E+16				1E+15	
shallow uniform donor density N_D ($1/cm^3$)		1.15E+17	1.2E+17		1E+15	1E+15
absorption constant A ($1/cm\ eV^{(½)}$)	9.6E+5	9.6E+5	9.6E+5		1E+5	1E+5
Defect type	Acceptor	Donor	Donor	Acceptor	Donor	
Capture cross section electrons (cm^2)	1E-15	1E-15	1E-15	1E-13	1E-15	
capture cross section holes (cm^2)	1E-12	1E-12	1E-12	1E-13	1E-12	
energetic distribution	Single	Single	Single	single	Single	
reference for defect energy level E_t	Above Ev	Above Ev	Above Ev	Above Ev of CdTe	Below Ec	
energy level with respect to Reference (eV)	0.090	0.090	0.090	0.10	0.2	
N_t total ($1/cm^3$) uniform	1E+14	1E+14	1E+14	1.00E+12	1E+14	

Table 2. Parameters for back and front contact

Parameters	Back contact	Front contact
surface recombination velocity of electrons (cm/s)	1.000E+5	1.000E+5
surface recombination velocity of holes (cm/s)	1.000E+7	1.000E+7
Metal work function (eV)	5	5.02
Majority Carrier barrier height relative to E_f (eV)	0.43	0.22
Majority Carrier barrier height relative to E_v (eV)	0.25	0



(a) (b)

Fig. 3. I-V curve for dark (red) and light (blue) condition for (a) thin film CdS/CdTe solar cell and (b) nw CdS/CdTe solar cell

Table 3. I-V characteristics of thin film CdS/CdTe solar cell and NW CdS/CdTe solar cell for temperature 300K

Results	Thin film CdS/CdTe SC	nw-CdS/CdTe SC
Open circuit voltage, V_{oc} (V)	0.69	0.82
Short circuit current, J_{sc} (mA/cm^2)	28.45	28.56
Fill Factor, FF (%)	78.96	78.06
Efficiency (%)	15.42	18.30

From table 3 we can realize that the use of CdS nanowires as window layer increases the efficiency by ~3%.

It is to be noticed from our results in Table 3 for Thin film CdS/CdTe SC and nw-CdS/CdTe SC that even though we have used planar and nanowire CdS layer of same thickness (0.1μm), greater V_{oc} and efficiency has been achieved when we used nanowires as window layer. This phenomenon occurs because unlike the solid planar CdS film, the nanowire CdS film has gaps between nanowires, which is transitive to sunlight photons. So, higher J_{sc} is obtained, resulting higher efficiency.

Also, in Table 1, we took higher effective bandgap for nw-CdS/CdTe SC than for Thin film CdS/CdTe SC, because these nanowires can be considered as stacks of tiny nano-discs. Thickness of these nano-discs are less than Bohr's radius of CdS (~4nm). So, quantum confinement effect of CdS nanowires can be attained which results in higher bandgap [7], [11].

When we considered CdS nanowires as window layer instead of thin film CdS, the junction area of CdS-CdTe interface decreased drastically because unlike thin film CdS-CdTe SC, junction happens only the tips of CdS nanowires in nw-CdS/CdTe SC. Thus, even though we have considered same parameters in the CdS-CdTe interface for both structures, interface recombination decreased for nw-CdS/CdTe SC, making the dark current very low. Consequently, a higher open circuit voltage, V_{oc} is obtained for nw-CdS/CdTe SC compared to that of thin film CdS/CdTe SC. This can be expressed by the following equation [7]:

$$V_{oc} = \left(\frac{AKT}{q}\right) \ln\left(\frac{I_L}{I_O} + 1\right) \quad (1)$$

The effective value of the diode ideality factor A is responsible for the improvement of the open circuit voltage. It is characterized by the ratio of the optical area, junction area and the dark current at the CdS–CdTe interface. The higher value of V_{oc} suggests that the efficiency of nw-CdS/CdTe SC is also greater than the efficiency of thin film CdS/CdTe SC.

In our work, our prime concern is to observe the effects of various parameters of nw-CdS/CdTe solar cell to attain high efficiency. Optimum values were chosen for every parameter for both thin film and nanowire CdS/CdTe solar cells. In the following section, various approaches are taken to enhance the efficiency of nw-CdS/CdTe solar cell. Parameters considered in Table 1 and Table 2 were varied for certain ranges and compared to the values used in Table 1 and Table 2 to secure high performance of nanowire CdS/CdTe solar cell.

The simulation of nw-CdS/CdTe solar cell is based on the experimental work of Hongmei Dang [7] where the efficiency was 12%. Higher conversion efficiency was achieved in our simulation structure. The efficiency was increased by ~6% as our numerical analysis provided an efficiency of 18.30%.

4. Effect of Various Parameters on Nanowire CdS/CdTe Solar Cell

4.1 Effect of temperature

The increase of temperature escalates the velocity of charged particles. In other words, the recombination rate of electrons and holes is increased. This results in reduced number of free electrons and holes. So, the efficiency decreases with increasing temperature.

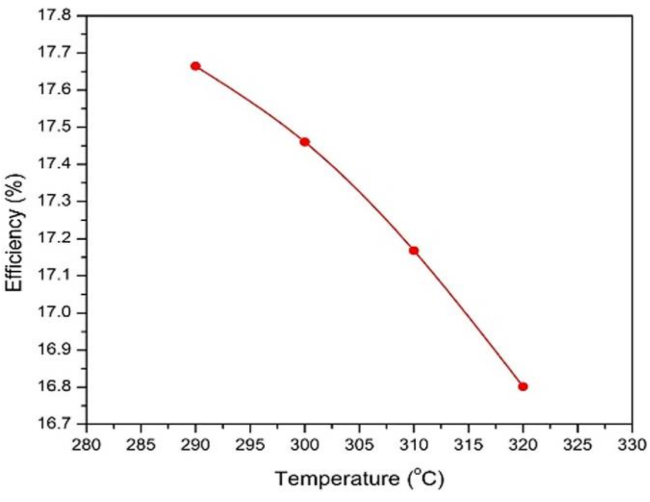


Fig. 4. Effect of temperature on nw-CdS/CdTe solar cell

Temperature coefficient describes the change of a physical property with the change of temperature which can be expressed as:

$$n(T) = n_0 + \alpha T \qquad (2)$$

Figure 4 shows the variation of efficiency with temperature. We have varied the temperature from 290K to320K and plotted against efficiency. The temperature coefficient was found to be varied from 0.06 to 0.05. As temperature coefficient, has varied a little with the temperature a linear relation is maintained.

4.2 Effect of interface state density

If the interface state density(N_{it}) between nw-CdS and CdTe layers is increases, the probability of finding electron is also increased at the interface. So, electrons are more likely to get captured there which leads to low Jsc. So, efficiency also decreases. To observe the effect of interface state density on I-V characteristics, the interface state density(N_{it}) between nw-CdS and CdTe layers were varied in the simulations from the range of $1x10^{12}$ $cm^{-2}$to $5x10^{13}$ cm^{-2}. It is seen from figure 5 that efficiency decreases rapidly when interface state density is increased. For N_{it} = $1x10^{12}cm^{-2}$ (blue curve), efficiency 18.30%. For N_{it} = $5x10^{12}cm^{-2}$(green curve), efficiency 10.44%. For N_{it} = $1x10^{13}cm^{-2}$(sky blue curve), efficiency 6.17% and for N_{it} = $5x10^{13}cm^{-2}$(pink curve), efficiency 0.90%. From the graphs, it can be realized that with the increase of N_{it}, short circuit current decreases which indicate the increase of reverse saturation current. Thus, overall decrease of solar cell efficiency is observed.

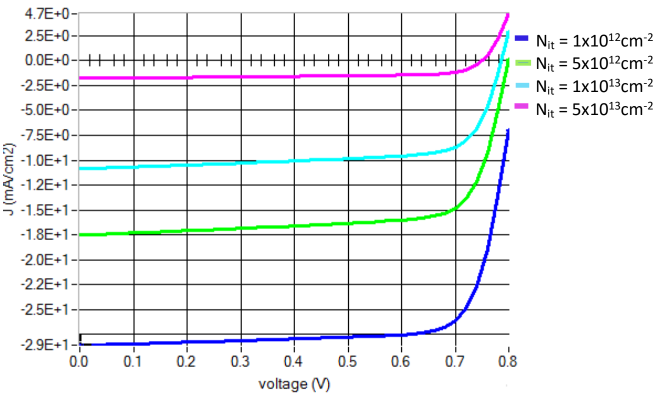


Fig. 5. Simulated light J-V curves of NW CdS/CdTe SC at various interface state densities

4.3 Effect of interface surface recombination velocity

The surface recombination velocity for electrons and holes at the interface is given by:

$$S_{(n,p)} = \sigma_{(n,p)} v_{th} N_{it} \qquad (3)$$

Where, N_{it}, v_{th}, $\sigma_{(n,p)}$ indicates density of interface traps, thermal velocity and capture cross section of holes and electrons, respectively.

The defects within the interface surface plays a vital role in monitoring the surface recombination velocity. The faster the electrons and holes of the interface are captured, the higher is the surface recombination velocity $S_{(n,\,p)}$ [12]. Since the rate of recombination on the surface is increased, an adverse effect on the efficiency of solar cell can be noticed. To ensure this, simulations were performed for a range of $1x10^6$ to $1x10^7$ cm/s. In Figure 6, for $S_{(n,p)}$ = $1x10^6$ cm/s, efficiency 18.30%.

For $S_{(n,p)} = 5x10^6$ cm/s, efficiency 14.90%. For $S_{(n,p)} = 1x10^7$ cm/s, efficiency 12.39%.

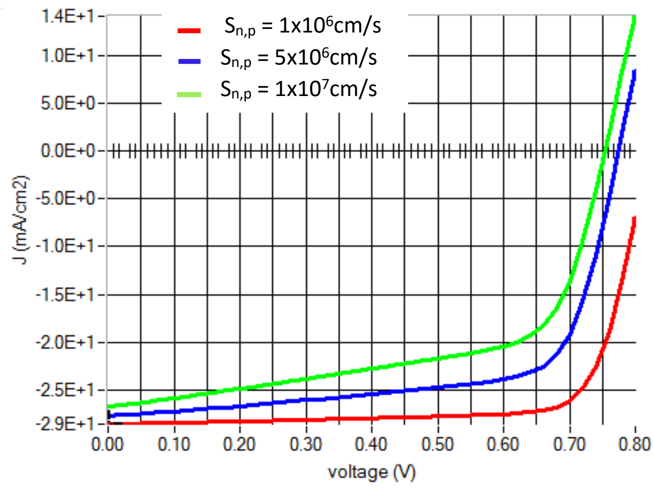


Fig. 6. Simulated I-V curves of nw-CdS/CdTe SC at various interface recombination velocity

4.4 Effect of effective density of states

Increase of N_c means increase of electrons in a n-type material and increase of N_v means increase of holes in a p-type material. It means reverse saturation current also increases. So, the open circuit voltage will decrease which will make the efficiency low. We varied the N_v of CdTe layer from $9x10^{18}cm^{-3}$ to $9x10^{21}cm^{-3}$ and N_c of CdS layer from $9x10^{18}$ cm^{-3} to $9x10^{19}cm^{-3}$. In figure 7 we see that, for p-type CdTe layer, increased number of holes are responsible for degrading V_{oc}, Thus the efficiency becomes lower than the prior result. Also, for n-type CdS layer, the lower the value of N_c, lower the electron to hole density ratio, which leads to higher V_{oc}, making the efficiency higher than before.

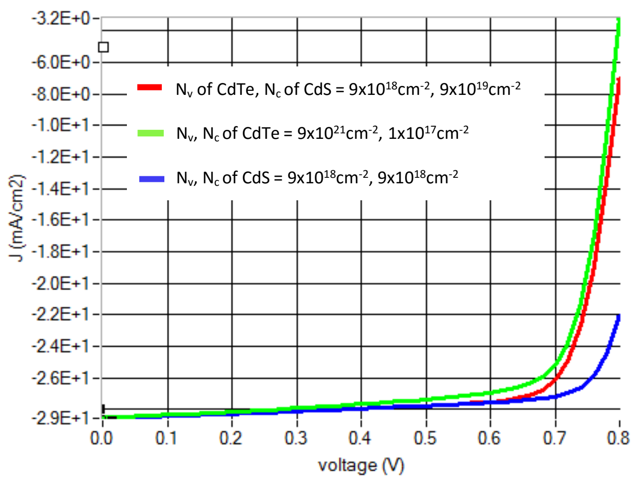


Fig. 7. Effect of effective density of states on nw-CdS/CdTe SC

Table 4. Effect of effective density of states

	Red curve	Green curve (Effect of Nv)	Blue curve (Effect of Nc)
Nv of CdTe layer(cm^{-3})	$9x10^{18}$	$9x10^{21}$ ↑	$9x10^{18}$
Nc of CdTe layer(cm^{-3})	$1x10^{17}$	$1x10^{17}$	$1x10^{17}$
Nv of nw-CdS layer(cm^{-3})	$9x10^{18}$	$9x10^{18}$	$9x10^{18}$
Nc of nw-CdS layer(cm^{-3})	$9x10^{19}$	$9x10^{19}$	$9x10^{18}$ ↓
Efficiency (%)	18.30	7.67 ↓	19.71 ↑

The results indicate that the efficiency decreases with the increase of N_v of CdTe layer or N_c of nanowire CdS layer.

4.5 Effect of metal work function

In the photoelectric effect, the work function is defined as the minimum amount of energy or photon needed to eject an electron from the surface of a metal. Since p-type CdTe have high electron affinity, fermi level pinning would occur at the interface of back contact and absorption layer. So, an energy barrier for electrons and holes would form by band bending at the metal-semiconductor interface. This would hamper the hole's transport and thus degrades the performance of solar cell [5]. Since schottky type back contact has a schottky barrier and does not allow carrier transport, ohmic contact is needed due to its non-rectifying behavior. Simulations have been done using silver (Ag), iron (Fe), niobium (Nb), copper (Cu) graphite alloy, nickel (Ni) and platinum (Pt). For higher metal work function, the majority carrier barrier height (relative to E_f) decreases, which means the contact gets more ohmic. As the work function of the metal increases, the V_{oc} gets increased. Thus, the efficiency of nw-CdS/CdTe solar cell also increases.

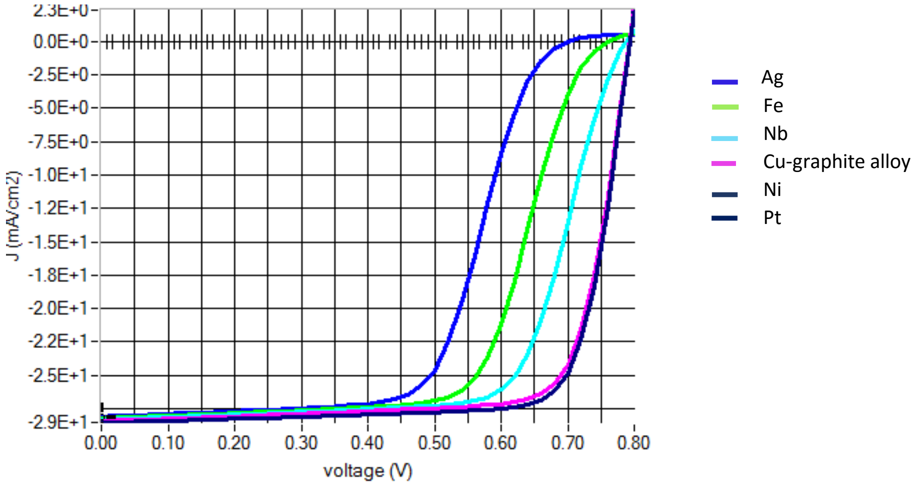


Fig. 8. Effect of metal work function on I-V characteristics on nw-CdS/CdTe

Table 5. Effect of metal work function on I-V characteristics

Back contact material	Ag	Fe	Nb	Cu-graphite alloy	Ni	Pt
metal work function, Φ_m (eV)	4.74	4.81	4.87	5.00	5.50	5.70
Efficiency (%)	12.56	14.37	15.92	18.30	18.70	18.70

From the Table 5 it can be concluded that efficiency increases with the increase of metal work function.

4.6 Rollover effect

Due to rollover effect, an I-V curve shows a bend at higher voltage, displaying a saturation like behavior. To explain rollover effect, it can be assumed that the back-contact acts as a rectifying Schottky contact which remains reverse biased with the CdS/CdTe solar cell. This phenomenon is known as two diode model [13].

One diode is formed between the interface of p-type CdTe and n-type CdS layer and the other diode is between the metal back contact and p-type CdTe layer. From the C-V curve of figure 9, for barrier height 0.6 Ev, it can be noticed that back contact limits the current at high forward bias [14]. It was realized that capacitance does not increase equivalently with voltage. Initially, capacitance increases with the increase of voltage and reaches to a maximum point. Then it drops sharply and reaches to a second maxima. Since the current is much

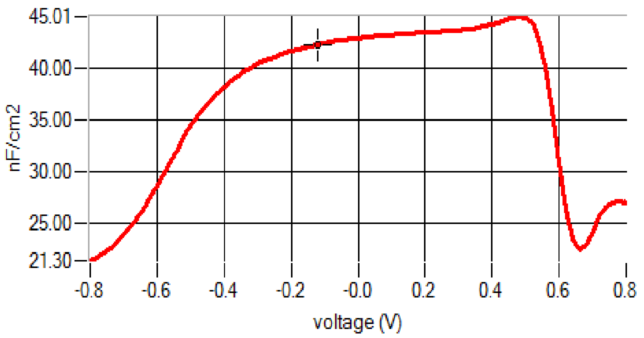


Fig. 9. C-V curve of nanowire CdS/CdTe solar cell at forward voltage

lower than the saturation current for low voltage, the entire voltage drops at the CdTe/CdS interface. Thus, the measured capacitance is the junction capacitance (for CdTe/CdS interface). At the intervening voltage, the voltage drop is divided among metal/CdTe interface and CdTe/CdS interface. The capacitance is sum of the junction capacitance and contact capacitance (for metal/CdS interface). For high voltage, current is restricted to the saturation current at contact and thus the extra voltage drops at the metal/CdTe interface. So, almost the entire capacitance is the contact capacitance which decreases with the increase of voltage, giving a slope of $1/C(V)^2$ [15]. This measurement of CdTe doping density both near CdTe/CdS interface and metal/CdTe interface and the presence of maxima indicates the presence of contact barrier. Therefore, a Schottky diode like behavior becomes noticeable between the surface of p-CdTe and back contact, for which performance of nw-CdS/CdTe solar cell degrades. This rollover effect becomes obvious when crooked I-V curves are found.

Simulations were performed to support the two-diode model. The barrier height, E_f (energy difference between the metal Fermi Level and the top of the valence band) was varied from 0.4 eV to 0.7 eV. For the barrier height of 0.4eV, V_{oc} = 0.82V, Jsc =28.56mA/cm^2, Fill Factor = 78.48% and Efficiency 18.42%. For the barrier height of 0.5eV, V_{oc} = 0.81V, Jsc =28.50mA/cm^2, Fill Factor = 74.67% and Efficiency 17.36%. For the barrier height of 0.6eV, V_{oc} = 0.78V, Jsc =28.37mA/cm^2, Fill Factor = 66.41% and Efficiency 14.89%. For the barrier height of 0.7eV, V_{oc} = 0.69V, Jsc =28.23mA/cm^2, Fill Factor = 62.77% and Efficiency 12.31%.

As we can see from Fig. 10, rollover effect arises for higher values of the barrier height (E_f). These bent I-V curves of low efficiencies suggest us to use back contact of lower E_f for avoiding rectifying Schottky contact.

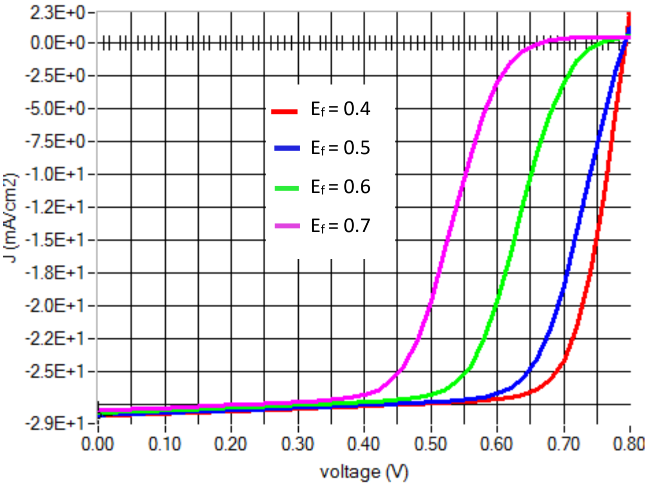


Fig. 10. Rollover effect on I-V characteristics on nw-CdS/CdTe SC

5. Conclusion

The thin film CdS/CdTe solar cell and nw-CdS/CdTe solar cell, both are simulated using SCAPS-1D and it is evident that nanowire CdS layer is more advantageous than planar CdS in solar cell. By using optimum values of required parameters for numerical analysis, a nw-CdS/CdTe SC of high efficiency (18.30%) was modeled. Several parameters were varied for observing I-V characteristics. From FDTD solutions for CdS nanowire it can be surmised that scattering is comparatively low for smaller diameters and higher wavelengths. The nw-CdS/CdTe solar cell was studied by using SCAPS-1D to evaluate the parameters responsible for the efficiency of this solar cell. From simulation, it can be deduced that efficiency of nw-CdS/CdTe solar cell can be increased by increasing density of states of p-type CdTe layer, metal work function and by decreasing temperature, interface state density, interface surface recombination velocity, density of state of CdS layer. To explain the rollover effect the back to back diode model have been considered and the results indicate that rollover effect becomes notable for higher barrier heights.
For further advancement, the ITO/i-SnO_2 combination can be superseded by Cd_2SnO_4/$ZnSnO_4$ combination [5]. A layer of quantum dots can be produced above the nanowire layer to enhance efficiency and to make it feasible enough for mass production and a competent alternative to current solar cell technology.

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