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Analysis of Voltage Gain Tolerance due to the Resonant Circuit Variation of LLC Resonant Converter

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Abstract- The LLC converter is an attractive solution for high power application, hence many photovoltaic systems which use LLC converter have been proposed. It is important on mass production stage to clarify the relationship between design parameters and its voltage gain tolerance which is caused by component variations. This issue is especially important for systems whose LLC converter is directly connected to photovoltaic panels, because there is no boost converter which can compensate insufficient voltage gain of the LLC converter. However the voltage gain tolerance of the LLC converter has rarely studied. Therefore we researched the relationship between the voltage gain tolerance and three normalized parameters which are related to the resonant circuit by Monte Carlo analysis. As a result, it has found that there is a linear area where voltage gain tolerance becomes to be small in quality factor – inductance ratio plane. By utilizing this knowledge, designers can reduce unnecessary losses of the LLC converter which are generated by too much voltage gain margin, therefore this paper can contribute to improving performance in renewable energy generation systems.

Keywords LLC converter; voltage gain; tolerance; Monte Carlo analysis.

1. Introduction

Recently the destruction of the environment is a serious problem. The renewable energy has been widely recognized as one of the most effective solutions of the problem, and the solar energy generation is an important energy source among the renewable energy sources. There are some studies which use LLC converter in photovoltaic systems [1–6], and it is a common issue to design the LLC converter to keep its performance with sufficient output voltage when values of resonant circuit components vary in the field. This issue is particularly important for the photovoltaic system whose LLC converter is directly connected to photovoltaic panels [2,4], because there is no boost converter which can compensate too small voltage gain of the LLC converter. However the relationship between the voltage gain tolerance and resonant circuit component variations has rarely studied.

Yang, Dubus and Sadarnac [7] analyzed the current balancing of two LLC converters using Monte Carlo analysis, however the voltage gain tolerance of a single LLC converter is not shown. Binder, Oeder, Barwig and Duerbaum [8] shows the design procedure of the LLC converter which takes component variations into account. However they show the design algorithm by flowchart, therefore the combination of the design parameters which makes the voltage gain tolerance to be small is not clear.

Because the rigorous voltage gain formula of the LLC converter is not obtained yet, a formula obtained by first harmonic approximation is generally used [9-11]. It is known that this approximation formula is not accurate when normalized frequency is much smaller then unity [12], therefore we do not use this formula in this study. We use a circuit simulator to analyze a voltage gain.

All the combination of three normalized parameters which are related to resonant circuit are used to analyze the voltage gain tolerance, because we think it is insufficient to change only one parameter at a time to know the relationship between the voltage gain tolerance and design parameters. As a result, it has found that there is a linear area where voltage gain tolerance becomes small in quality factor – inductance ratio plane. We name this area 'voltage gain tolerance valley'. This valley affects the design of the LLC converter to minimize the voltage gain tolerance. This paper presents the design method to minimize the voltage gain tolerance, and designers can reduce unnecessary losses which is caused by too much voltage gain margin.

2. Procedure of Analysis

2.1. Target Converter and Definition of Symbols

The target converter for the analysis in this paper is shown in Fig. 1.

The normalized parameters and its symbols defined in Table 1 are used in this paper to have general versatility.

2.2. Viewpoints of Analysis

The problems caused by variations in the resonant circuit components are the following two cases.

(I) V_{OUT} is too low at a rated power and minimum V_{IN}.

(II) V_{OUT} is too high at no load and maximum V_{IN}.

The voltage gain of the LLC converter obtained by first harmonic approximation is known as Eq. (1) [11]. By assigning zero to Q and infinite to f_N, M in case (II) is calculated as Eq. (2). Related parameter in Eq. (2) is only L_N, therefore detailed analysis is not required in case (II).

From the above, the analysis in this paper is performed considering only case (I).

$$M=\frac{1}{\sqrt{\left(1+L_N-\frac{L_N}{f_N{}^2}\right)^2+Q^2\left(f_N-\frac{1}{f_N}\right)^2}} \tag{1}$$

$$M=\frac{1}{1+L_N} \tag{2}$$

2.3. Procedure of Analysis

We use normalized parameters for input and output parameters of the analysis, however varying parameters in the field are real values such as inductance or capacitance. Therefore the analysis is performed in following steps. Step 5 is necessary to make the output power to be constant. The circuit simulator used in this analysis is SCAT (Switching Converter Analysis Tool) [13].

1. Calculate C_R from n, f_R, Q and R_{OUT} using Eq. (3).
2. Calculate L_R from C_R and f_R using Eq. (4).
3. Calculate L_M from L_R and L_N using Eq. (5).

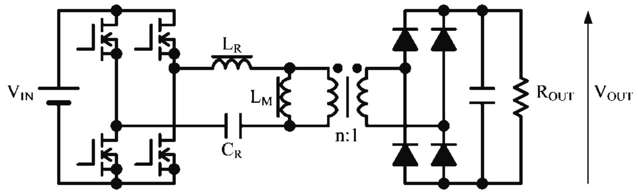


Fig. 1. LLC resonant converter.

Table 1. Definition of symbols.

C_R	Resonant capacitor and its capacitance
L_R	Resonant inductor and its inductance
L_M	Magnetizing inductor of transformer and its inductance
n	Transformer turns ratio: primary turns/secondary turns
R_{OUT}	Load resistance
R_{AC}	Reflected R_{OUT}: $8n^2/\pi^2{*}R_{OUT}$
Z_O	Characteristic impedance: $\sqrt{(L_R/C_R)}$
V_{IN}	Input voltage
V_{OUT}	Output voltage
M	Voltage gain: nV_{OUT}/V_{IN}
L_N	Inductance ratio: L_R/L_M
Q	Quality factor: Z_O/R_{AC}
f_{SW}	Switching frequency
f_R	Resonant frequency: $1/(2\pi\sqrt{(L_RC_R)})$
f_N	Normalized switching frequency: f_{SW}/f_R

4. Create samples which have a normal distribution with a predetermined standard deviation and typical value calculated in step 1 to 3 using a random number.
5. Set typical value of C_R, L_R and L_M to the component of the circuit simulator and regulate V_{IN} to have specified V_{OUT}.
6. Set each value of the sample set to the component of the circuit simulator.
7. Calculate voltage gain M from V_{IN}, n, and V_{OUT} whose value is obtained from circuit simulation in steady state.
8. Calculate standard deviation from obtained set of M, and calculate tolerance of M from standard deviation.

Eq. (3) – (5) are obtained from definitions of normalized parameters.

$$C_R=\frac{\pi}{16n^2 f_R Q R_{OUT}} \tag{3}$$

$$L_R=\frac{1}{C_R}\left(\frac{1}{2\pi f_R}\right)^2 \tag{4}$$

$$L_M=\frac{L_R}{L_N} \tag{5}$$

2.4. Parameters used in Analysis

Circuit parameters used in the analysis are shown in Table 2. Considering case (I), f_N is a minimum value which is limited by a controller. Therefore its values are selected to be lower than unity. The values of Q and L_N are assumed to be used generally. The values of n, V_{OUT} and R_{OUT} are assumed for a converter whose output is 380V 20A, 54V 140A and 14V 270A.

Parameters related to the Monte Carlo analysis are shown in Table 3. All tolerances of L_R, L_M and C_R are assumed to be ±7% and they correspond to ±3 times of standard deviation. The voltage gain tolerance also corresponds to ±3 times of standard deviation. The number of samples is one thousand. Therefore analysis using prototype converters is difficult and a feasible method is simulation only. Even if the result of one combination of parameters is required, one thousand samples are necessary too, therefore analysis using prototype converter is impossible practically.

3. Result of Analysis

The results of the analysis are shown from Fig. 2 to Fig. 4. The analysis result of a converter which is assumed to have 380V 20A output is shown in Fig. 2, 54V 140A output is shown in Fig. 3 and 14V 270A output is shown in Fig. 4. The Z axis of these graph means the voltage gain tolerance, and 2% step size of the Z axis corresponds to the contour line. Each graph shows how voltage gain tolerance changes by the combination of typical value of the inductance ratio and the quality factor. The variation from (a) to (h) means the change of minimum normalized frequency which is limited by a controller.

The difference between Fig. 2 and Fig. 3 is an output voltage, and the difference between Fig. 2 and Fig. 4 is an output voltage and an output power. Regardless of the difference above, the analysis result is exactly similar. The same result is obtained when f_R is changed to 50kHz and 150kHz, however the results are not be shown here because there is not enough space. Based on the analysis results above, it is reasonable to suppose that the analysis result of Fig. 2 is applicable for the converter which has another specification and another design, therefore it has general versatility.

Table 2. Circuit parameters used in analysis.

Q	0.20, 0.25, 0.30, … , 0.90, 0.95, 1.00
L_N	0.100, 0.125, 0.150, … , 0.450, 0.475, 0.500
f_N	0.50, 0.55, 0.60, 0.65, 0.70, 0.75, 0.80, 0.85
f_R	100kHz
n	1 / 7 / 27
V_{OUT}	380V / 54V / 14V
R_{OUT}	19Ω / 0.386Ω / 0.0519Ω

Table 3. Parameters for Monte Carlo analysis.

Number of samples	1,000
Tolerance of C_R, L_R and L_M	±7%
Tolerance above / standard deviation	3
Voltage gain tolerance / standard deviation	3

There is a linear area where voltage gain tolerance becomes small in quality factor – inductance ratio plane, that is 'voltage gain tolerance valley'. The shape of the valley is a downward-sloping line in quality factor – inductance ratio plane, and it moves toward origin when f_N becomes to be smaller value. The left side of the valley covers all the area in the graph when f_N is equal to 0.85, however the right side of the valley covers almost all area when f_N is equal to 0.5.

Designers should select the best combination of design parameters which minimize the voltage gain tolerance and which provides a required voltage gain. The voltage gain tolerance valley affects this selection of the combination of design parameters, and it is shown in the design example below.

3.1. Influence of Normalized Frequency

Lower f_N makes both minimum and maximum voltage gain tolerance to be larger value. It means that the voltage gain tolerance of LLC converter becomes to be large in case (I) when a range of V_{IN} and/or V_{OUT} is wide, because minimum f_N of such converter is low.

3.2. Influence of Inductance Ratio

Lower inductance ratio makes the voltage gain tolerance to be small at the left side of the valley, however the tolerance is independent from inductance ratio at the right side of the valley. The combination of the design parameter should be selected from left side of the valley or the valley itself, because the tolerance is large at the right side of the valley.

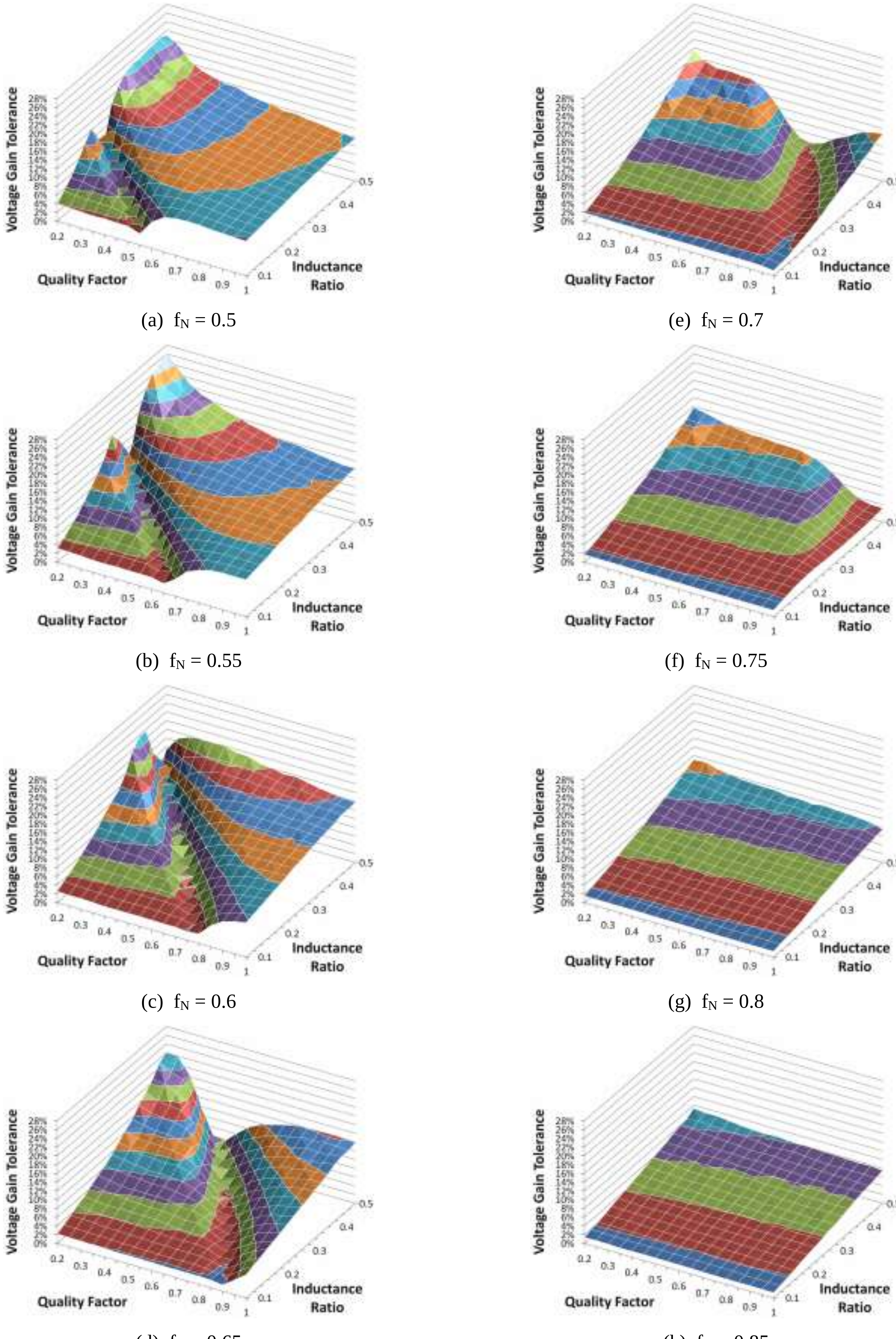
It means that the voltage gain tolerance of LLC converter becomes to be large in case (I) when a range of V_{IN} and/or V_{OUT} is wide, because Eq. (2) constrains the inductance ratio to be large value.

3.3. Influence of Quality Factor

The voltage gain tolerance is independent from quality factor at the left side of the valley, and higher quality factor makes the tolerance to be small at the right side of the valley. The design parameters which can control the voltage gain tolerance are quality factor and normalized frequency, because they are not constrained by environmental condition.

3.4. Design Example using Result of Analysis

By using design constraint and the analysis result shown in Fig. 2, designers can find the design parameter which



(a) $f_N = 0.5$

(e) $f_N = 0.7$

(b) $f_N = 0.55$

(f) $f_N = 0.75$

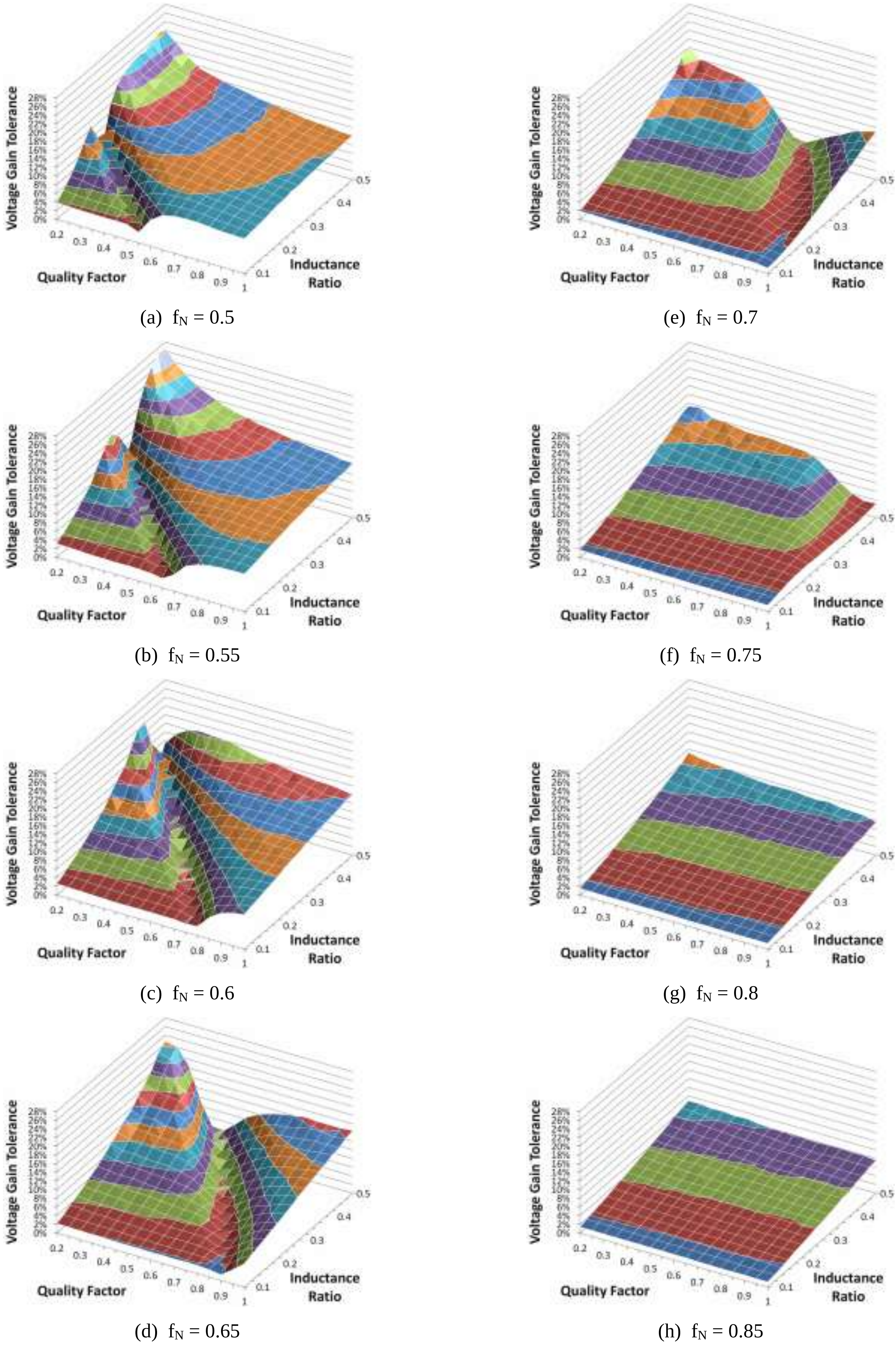
(c) $f_N = 0.6$

(g) $f_N = 0.8$

(d) $f_N = 0.65$

(h) $f_N = 0.85$

Fig. 2. Voltage gain tolerance versus quality factor and inductance ratio (380V20A).



(a) $f_N = 0.5$

(b) $f_N = 0.55$

(c) $f_N = 0.6$

(d) $f_N = 0.65$

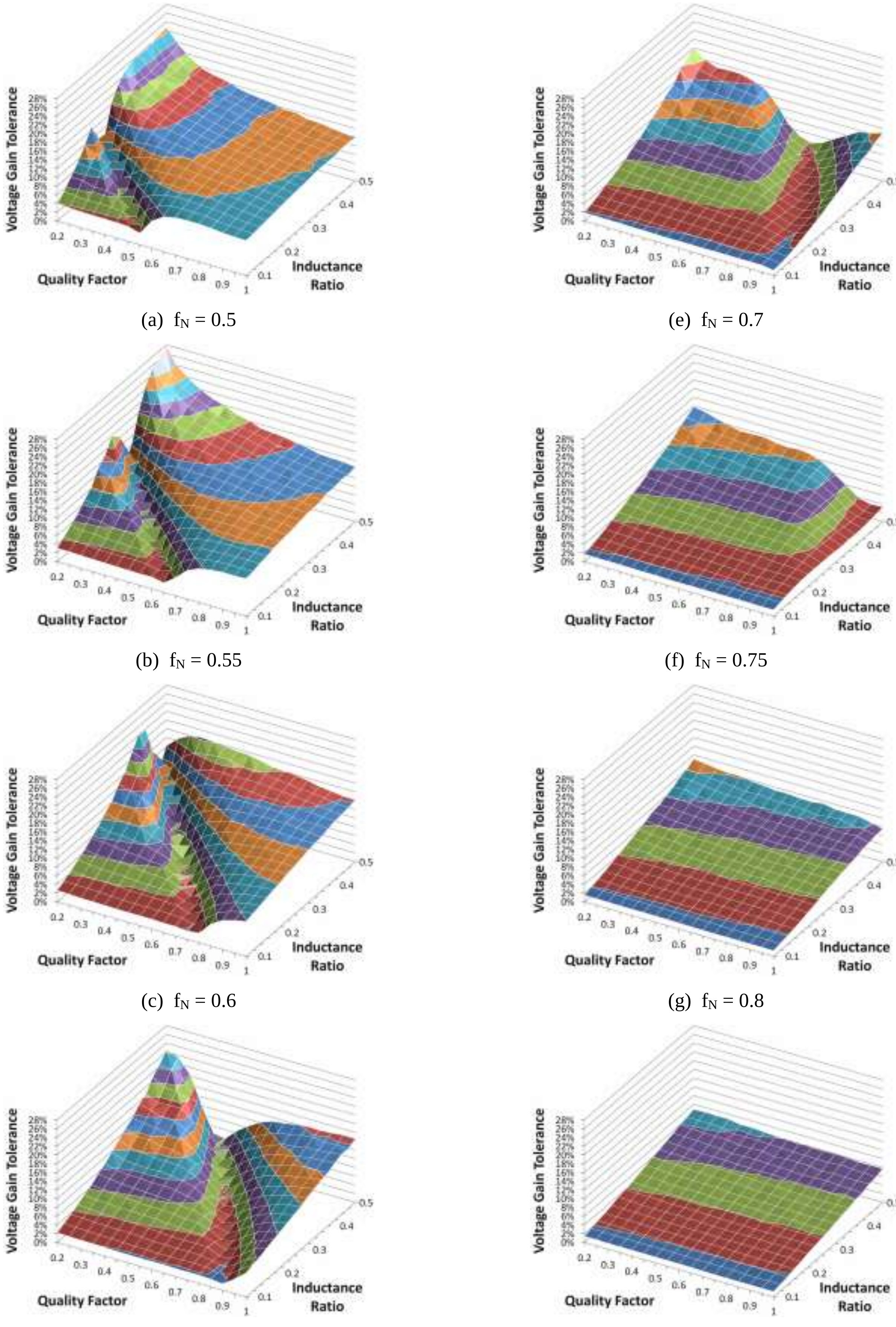
(e) $f_N = 0.7$

(f) $f_N = 0.75$

(g) $f_N = 0.8$

(h) $f_N = 0.85$

Fig. 3. Voltage gain tolerance versus quality factor and inductance ratio (54V140A).



(a) $f_N = 0.5$

(e) $f_N = 0.7$

(b) $f_N = 0.55$

(f) $f_N = 0.75$

(c) $f_N = 0.6$

(g) $f_N = 0.8$

(d) $f_N = 0.65$

(h) $f_N = 0.85$

Fig. 4. Voltage gain tolerance versus quality factor and inductance ratio (14V270A).

minimize the voltage gain tolerance. The constraint condition example is 'minimum $f_N = 0.5$ and $M > 2$'. Figure 5 shows a contour map of the voltage gain at $f_N = 0.5$, and Fig. 6 shows a contour map of the voltage gain tolerance at $f_N = 0.5$. It is found from Fig. 5 and Fig. 6 that in $M > 2$ region, minimum voltage gain tolerance is obtained at $Q = 0.35$ and $L_N = 0.2$. Therefore this is the best selection if it meets a case (II) constraint, and 5.28% voltage gain tolerance is obtained.

4. Conclusion

This paper shows the relationship between normalized design parameters of the LLC converter and its voltage gain tolerance which is caused by resonant circuit component's variation. The results of the analysis are very similar in different output voltage, different output power and different resonant frequency, therefore it is reasonable to suppose that this result has general versatility. The analysis is performed using a circuit simulator and Monte Carlo method.

The result of the analysis clarifies that there is a linear area where voltage gain tolerance becomes to be small in quality factor – inductance ratio plane, named 'voltage gain tolerance valley'. The combination of the design parameter should be placed in this valley to minimize the voltage gain tolerance. The design example which uses the analysis result and design constraint is shown in this paper. By using this design method, designers can reduce unnecessary losses which are caused by too much voltage gain margin.

The result of the analysis and the design method shown in this paper is particularly important for photovoltaic system which has the LLC converter and no boost converter, because insufficient voltage gain of the LLC converter is not compensated by boost converter. Therefore this paper can contribute to improving performance in renewable energy generation systems.

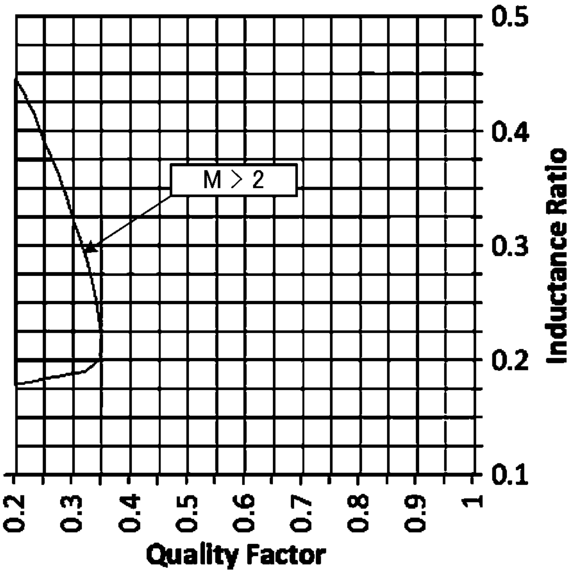


Fig. 5. Region where $f_N = 0.5$ and $M > 2$.

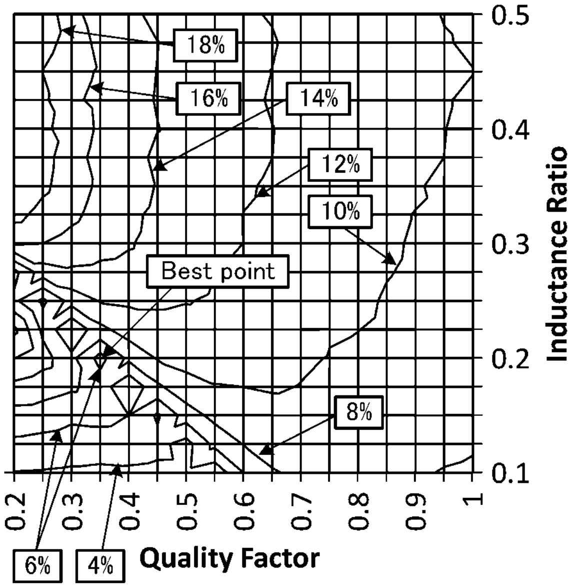


Fig. 6. Contour map of $f_N = 0.5$ and best design point.

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