High step-down Dual Output Light Emitting Diode Driver

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Abstract- A conventional power factor correction (PFC) based light emitting diode (LED) drivers composed of two-stage DC-DC conversions has several drawbacks such as; increased system size due to more component count, less efficiency and complex control etc. The grid powered LED lighting demand for high step-down conversion because the required voltage level of LED light is very less. Thus, this work proposes a one-switch dual-output (OSDO) coupled-inductor buck (CIB) LED driver. The OSDO-CIB converter can eliminates the drawbacks of conventional counterparts. The proposed OSDO-CIB converter can provide various benefits such as; compact size, high efficiency, less total harmonic distortion (THD), simple control, and a significant reduction in device voltage/current rating due to coupled inductors. The converter is designed with discontinuous conduction mode (DCM) of operation in order to achieve in-phase current and voltage, high power factor (PF) and a low THD. This paper mainly emphasized on detailed operating modes and steady-state analysis of proposed converter. Further, prototype of the converter is built and experimental validations are presented.

Keywords Coupled-Inductor (CI), Discontinuous conduction mode, Light Emitting Diode, Total Harmonic Distortion, Buck converter.

1. Introduction

Solid-state LEDs are used increasingly in lighting applications due to its significant advantages like; high brightness, longevity, absence of toxic-gas, energy-efficient and compact size [1, 2]. Due to longevity and energy efficient, LEDs are being widely used in various applications such as household, street, transportation, indoor lighting systems and LCD panels etc [3]. When LEDs are fed from utility grid an AC-DC converter is essential to provide regulated dc voltage to drive LED light. Also, to make the line current and the voltage in phase in order to achieve high PF with low THD which comply the IEC 61000-3-2 class C standards [4, 5].

Several authors have reported different types of passive and active PFC techniques to achieve high PF with low THD. A passive PFC technique provides low electromagnetic interference (EMI) due to supply frequency operation and achieves high efficiency. However, due to line frequency design of magnetic components (inductors and transformers) and capacitors results in bulky size and weight [6, 7]. An active PFC technique (switching converter) provides high PF, less THD and high efficiency. Fig. 1(a) shows the conventional two-stage active PFC circuit consists of PFC pre-regulator followed by the DC-DC converter. Thus, two-stage PFC technique needs more components, which increase converter size significantly. In addition, control complexity increases and system efficiency decreases [8, 9]. Fig. 1(b) shows the single-stage PFC circuit that provides both PFC operation and regulation of output voltage. Since cost is a major aspect, single-stage PFC-based LED drivers with simple control technique leads to compact size, high efficiency and hence, it is an attractive choice for low power lighting applications.

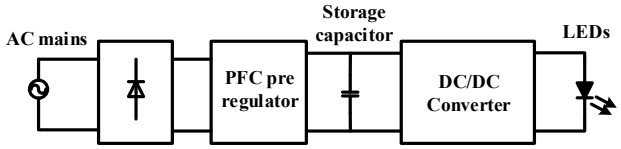


Fig. 1 (a) Classical two-stage LED driver

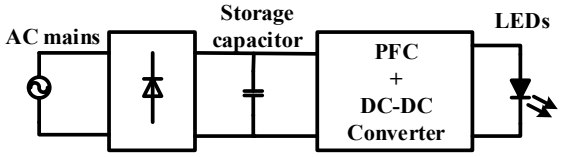


Fig. 1 (b) Single-stage LED driver

Now a days, most of the research is departing on single-stage PFC LED drivers with PF greater than 0.9 and low THD. An apt review of PFC converter topologies is reported [10, 11]. For low power applications single-stage buck based PFC topologies are preferable due to its simple structure and low component count [12-14]. However, the efficiency decreases significantly when the high step-down conversion is desired for the low power LED lighting system. In addition, conventional buck converter suffers from high device (voltage/current) stress during high step-down operation. However, a coupled inductor (CI) configuration can reduce the device (voltage/current) stress during high step-down operation in contrast to classical buck converter of same power rating.

A few other topologies reported in the literature shows numerous benefits such as; high step-down conversion ratio, less off-state voltage/on-state current of the switching devices with single output only [15-19]. B L et al. [15] proposed bi-directional CI buck-boost converter with a high step up/down conversion ratio. Although two switches are required for both step up/down conversion, its structure is suitable only for single output when operated as a step up/down. In [16] a single-stage bridge less AC-DC converter to supply power for plasma display panels, but its size and cost would be high due to more component counts. Lee et al. [17] presented an active zero voltage switching (ZVS) CI step-down converter, but as it involves auxiliary switching circuit to achieve ZVS which makes the circuit complex and hence, higher cost. MA et al. [18] reported a valley-fill single ended primary inductance (SEPIC) converter without electrolytic capacitors. However, for single-output it involves high components. KI et al. [19] reported buck integrated buck-boost converter with low switch voltage stress. Nevertheless, for single-output it involves two inductors and three fast diodes can increase the cost and size. Single inductor multi-output buck converter topologies are reported [20, 21], but it leads to increased size and cost of overall system due to high device count. Luo et al. [22] proposed multi-output step-down converter and it requires additional switch and capacitor for each output. In [23] bridgeless multi-output using SEPIC converter is reported which leads to high conduction losses. These aforementioned issues motivate to design a cost effective and compact size PFC-based dual-output converter for lighting applications. Therefore, this work proposes an OSDO-CIB PFC converter with less component count and high step-down conversion ratio. The proposed topology simplifies the gate-driver complexity by connecting the source terminal of the main switch to ground potential while retaining the benefits of classical CIB converter counterparts such as high step-down conversion, reduction in current/voltage stress on switch/diode and high efficiency. The converter is designed to operate in discontinuous conduction mode (DCM) to attain high PF and low THD which comply with the IEC 61000-3-2 class C standards. Further, a prototype of the converter is built and experimental validations are presented.

Due to the energy deficiency and environmental problems, the renewable energy sources (RES) have gaining more importance [24]. The power generated from RES can be connected to grid through proper converter. Further, the stand alone systems are required to supply the load power when RES are unavailable [25]. Most commonly buck derived converters are used for battery charge application due to its simplicity and low component count. Generally, the battery output voltage is lower than the voltage generated from RES. Therefore, the conventional buck converters are preferred for the high input and low output voltage applications. However, the efficiency decreases when the high step-down conversion is desired due to poor utilization of the switch (less duty ratio) at the peak value of input voltage. In order to overcome the limitations of conventional buck converter for the high input and low output voltage applications the coupled-inductor buck converter would be a preferred choice for such RES integrated energy storage system. Hence, proposed converter would be a viable and attractive for renewable energy applications.

2. Operation and Design Analysis

Fig. 2 illustrates the proposed grid fed LED driver which consist of front-end rectifier followed by PFC-based OSDO-CIB converter. The main feature of the proposed OSDO-CIB converter is simple in its structure due to less component count (i. e. only one MOSFET switch, two diodes and two CIs). The major symbols used in a proposed circuit are summarized as follows; V_{in} (I_{in}) and v_{dc} are ac source voltage (current) and the average value of rectified voltage respectively. V_{o1} (I_{o1}) and V_{o2} (I_{o2}) are output voltage (current) of load-1 and load-2 respectively. L_f and C_f are filter inductor and capacitor at ac source side respectively. C_{o1} and C_{o2} are output filter capacitors of load-1 and load-2 respectively. L_{P1} (L_{S1}) primary (secondary) inductances of T_1 and L_{P2} (L_{S2}) are primary (secondary) inductances of T_2. The MOSFET switch is represented as S; the freewheeling diodes are represented as D_1 and D_2 respectively. The R_{o1} and R_{o2} are equivalent resistances of the load-1 and load-2 respectively and both the loads are identical. The CIs in Fig. 2 are identical and a replica of an ideal transformer with magnetizing inductance/s L_{mP1} (L_{mS1}) and L_{mP2} (L_{mS2}) and leakage inductance/s of L_{kP1} (L_{kS1}) and L_{kP2} (L_{kS2}) which is not shown in Fig. 2. The coupling parameters k_{P1} (k_{S1}), k_{P2} (k_{S2}) and turns ratio (N_1 & N_2) of the ideal transformer are defined as follows.

$$N_1 = \frac{N_{S1}}{N_{P1}},\ N_2 = \frac{N_{S2}}{N_{P2}},\quad \text{Where } N = N_1 = N_2 \tag{1}$$

$$k_{P1} = \frac{L_{mP1}}{L_{mP1} + L_{kP1}} = \frac{L_{mP1}}{L_{P1}}$$
$$k_{P2} = \frac{L_{mP2}}{L_{mP2} + L_{kP2}} = \frac{L_{mP2}}{L_{P2}} \tag{2}$$

$$k_{S1} = \frac{L_{mS1}}{L_{mS1} + L_{kS1}} = \frac{L_{mS1}}{L_{S1}}$$
$$k_{S2} = \frac{L_{mS2}}{L_{mS2} + L_{kS2}} = \frac{L_{mS2}}{L_{S2}} \tag{3}$$

Where N_{P1} (N_{S1}) and N_{P2} (N_{S2}) represents the winding turns in primary (secondary) of T_1 and T_2 respectively. In order to make (L_{mP1} = L_{P1}, L_{mP2}=L_{P2}) and (L_{mS1} = L_{S1}, L_{mS2}=L_{S2}) from (2) and (3) the coefficient of coupling is simply set to one (k_{P1}=k_{P2}=1 and k_{S1}=k_{S2}=1). The assumptions made for the analysis of proposed converter are as follows; (i) all the switching devices are ideal, (ii) zero conduction voltage drops of the switch and freewheeling diodes and (iii) inductor current is periodic under steady-state.

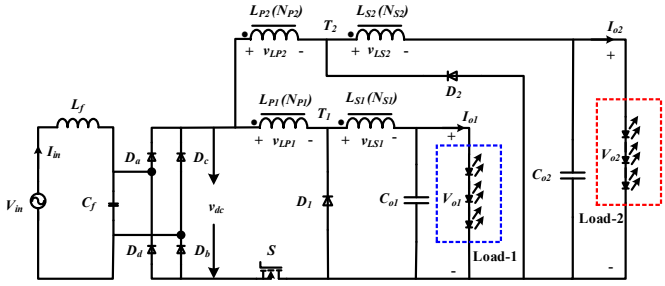


Fig. 2 Proposed PFC-based one-switch dual-output coupled-inductor buck converter.

2.1. Modes of operation

The OSDO-CIB converter is operating in DCM to achieve high PF with low THD. In DCM, the inductor current starts from zero in every cycle and hence, turn-on switching loss is zero. During off period the freewheeling diodes recover smoothly with finite di/dt because inductor energy resets completely well before the next switching cycle begins. Another significant feature of DCM is the required inductance value is small which results in the compact size of the converter. The main issue in DCM is high ripple current and hence, increases the device current ratings. However, for low power applications DCM is preferable. The equivalent circuits under each mode of operation and theoretical waveforms are shown in Fig. 3 and Fig. 4 respectively. The operating modes of OSDO-CIB converter in DCM are described as follows;

***Mode-1*:** The switch (S) is turned-ON for a δT_s period while freewheeling diodes D_1 and D_2 become reverse biased as shown in Fig. 3(a). In this mode, the rectified voltage v_{dc} supplies energy to the load-1 and load-2 through T_1 and T_2 respectively. The series combination of windings L_{P1} and L_{S1} of T_1, L_{P2} and L_{S2} of T_2 are energized and the current increases linearly. According to Kirchhoff's voltage law (KVL), the voltage v_{LS1} and v_{LS2} is given by

$$v_{LS1} = \frac{\left(v_{dc} - V_{o1}\right)N_1}{\left(1 + N_1\right)} \tag{4}$$

$$v_{LS2} = \frac{\left(v_{dc} - V_{o2}\right)N_2}{\left(1 + N_2\right)} \tag{5}$$

Mode-2: When S is turned-OFF, the D_1 and D_2 gets forward biased, and its equivalent circuit is shown in Fig. 3(b). During this mode, the current in i_{LP1} and i_{LP2} becomes zero and the secondary currents i_{LS1} and i_{LS2} will reset through freewheeling diodes. The voltage across the v_{LS1} and v_{LS2} are given by

$$v_{LS1} = -V_{o1} \tag{6}$$

$$v_{LS2} = -V_{o2} \tag{7}$$

***Mode-3*:** Fig. 3(c) shows the equivalent circuit of mode-3. This mode begins when windings L_{S1} and L_{S2} resets completely, and hence freewheeling diodes D_1 and D_2 gets reverse biased while the switch S is already in OFF position to ensure the DCM operation. During this interval the output filter capacitors C_{o1} and C_{o2} alone supplies power to load-1 and load-2 respectively until next switching cycle begins.

2.2. Voltage gain derivations

The DC gains of OSDO-CIB converter are discussed as follows. During DCM operation of the converter, the diode conduction period (δ_1) depends on the stored energy in the CIs. By using volt-second balance the average winding voltages v_{LS1} and v_{LS2} is zero over a switching period (T_S).

$$\frac{\left(v_{dc} - V_{o1}\right)N_1}{\left(1 + N_1\right)}\delta T_S - V_{o1}\delta_1 T_S = 0 \tag{8}$$

$$\frac{\left(v_{dc} - V_{o2}\right)N_2}{\left(1 + N_2\right)}\delta T_S - V_{o2}\delta_1 T_S = 0 \tag{9}$$

Where δ is duty cycle of the switch S. From (8) and (9), the dc gains (G_{Vo1} & G_{Vo2}) of proposed OSDO-CIB converter in DCM can be obtained as follows;

$$G_{Vo1} = \frac{V_{o1}}{v_{dc}} = \frac{\delta}{\delta + \delta_1\left(1 + 1/N_1\right)} \tag{10}$$

$$G_{Vo2} = \frac{V_{o2}}{v_{dc}} = \frac{\delta}{\delta + \delta_1\left(1 + 1/N_2\right)} \tag{11}$$

While operating the converter in DCM, the control variable is only δ whereas δ_1 is an only freewheeling interval which depends on stored energy in the CI. From Fig. 4 the average value of i_{LS1} and i_{LS2} can be defined as

$$i_{LS1(avg)} = \frac{1}{2} i_{LS1(\max)} \left[\delta + \delta_1\right] \tag{12}$$

$$i_{LS2(avg)} = \frac{1}{2} i_{LS2(\max)} \left[\delta + \delta_1\right] \tag{13}$$

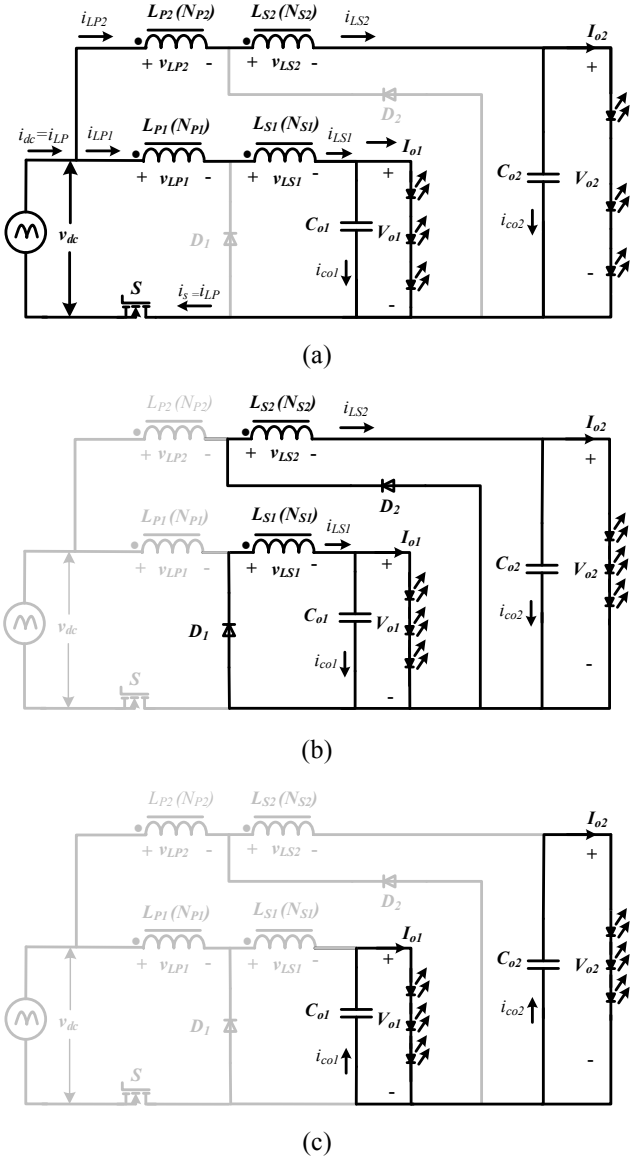


Fig. 3 Equivalent circuits of proposed OSDO-CIB converter; (a) Mode-1; (b) Mode-2; (c) Mode-3.

The maximum current in secondary windings of T_1 and T_2 can be expressed as

$$i_{LS1(\max)} = \left(V_{o1}/L_{S1}\right)\delta_1 T_S \tag{14}$$

$$i_{LS2(\max)} = \left(V_{o2}/L_{S2}\right)\delta_1 T_S \tag{15}$$

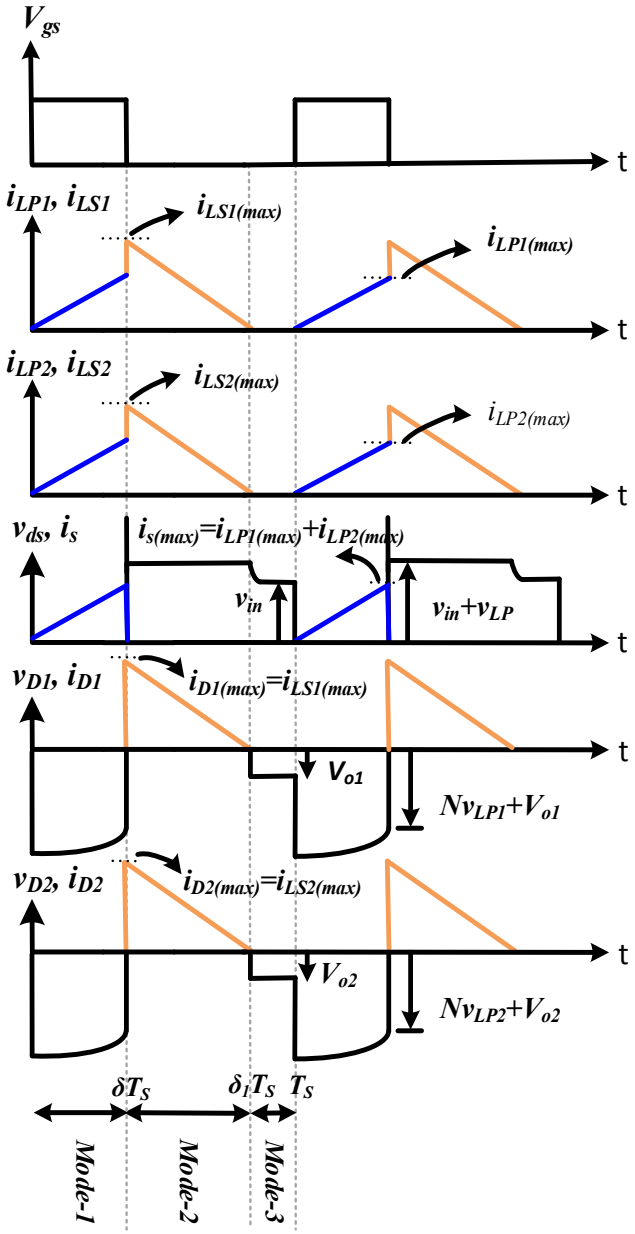


Fig. 4 Theoretical waveforms of proposed OSDO-CIB LED driver

By substituting (14) into (12), and (15) into (13), average currents are obtained as

$$i_{LS1(avg)} = \left(V_{o1}/2L_{S1}\right)\delta_1 T_S \left[\delta + \delta_1\right] \tag{16}$$

$$i_{LS2(avg)} = \left(V_{o2}/2L_{S2}\right)\delta_1 T_S \left[\delta + \delta_1\right] \tag{17}$$

Since $i_{Ls1\ (avg)} = I_{o1}$ and $i_{Ls2\ (avg)} = I_{o2}$, therefore we get

$$i_{LS1(avg)} = \left(V_{o1}/R_{o1}\right), \quad i_{LS2(avg)} = \left(V_{o2}/R_{o2}\right) \tag{18}$$

By simplifying (16) and (18), the δ_1 can be obtained as

$$\delta_1 = \frac{-\delta + \sqrt{\delta^2 + \left(8L_{S1}/R_{o1}T_S\right)}}{2} = \frac{-\delta + \sqrt{\delta^2 + \left(8L_{S2}/R_{o2}T_S\right)}}{2} \tag{19}$$

By substituting (19) into (10) and (11), the voltage gains M_{Vo1} and M_{Vo2} of proposed OSDO-CIB converter are obtained as follows;

$$G_{Vo1} = \frac{2}{\left(1-\frac{1}{N_1}\right)+\left(1+\frac{1}{N_1}\right)\left(\sqrt{1+\frac{8L_{S1}}{R_{o1}T_s\delta^2}}\right)} \tag{20}$$

$$G_{Vo2} = \frac{2}{\left(1-\frac{1}{N_2}\right)+\left(1+\frac{1}{N_2}\right)\left(\sqrt{1+\frac{8L_{S2}}{R_{o2}T_s\delta^2}}\right)} \tag{21}$$

By substituting N_1=0.2≈0.8 into (20) and N_2=0.2≈0.8 into (21) the curves of DCM voltage gains G_{Vo1} and G_{Vo2} with respect to δ are plotted as shown in Fig. 5(a) and Fig. 5(b) respectively. By analyzing Fig. 5, the turn's ratio N_1 and N_2 are selected as 0.5.

During switch S is ON the secondary inductor currents i_{Ls1} and i_{LS2} are charged for the δT_s period. During switch OFF period both the currents are freewheels through diodes D_1 and D_2. The charging and discharging intervals of both the secondary currents are equal because the both the loads are operating with single switch S with duty cycle (δ). In study state, neglecting switching frequency ripples and assuming average values of secondary currents of are $i_{LS1\ (avg)}$ and $i_{LS2\ (avg)}$.

$$\delta T_s i_{LS1(avg)} = \delta T_s i_{Ls2(avg)} \tag{22}$$

$$i_{LS1(avg)} = i_{Ls2(avg)} \tag{23}$$

2.3. Design considerations and device stress calculation

In continuous conduction mode (CCM), the minimum current carried by windings L_{S1} and L_{S2} are represented as

$$i_{LS1(\min)} = i_{LS1(avg)} - \frac{\Delta i_{LS1}}{2}$$
$$i_{LS2(\min)} = i_{LS2(avg)} - \frac{\Delta i_{LS2}}{2} \tag{24}$$

By substituting (4) and (5) into (24) under BCM $i_{Ls1\ (min)} = 0$ and $i_{Ls2\ (min)} = 0$; the minimum value of L_{s1} and L_{s2} are represented as;

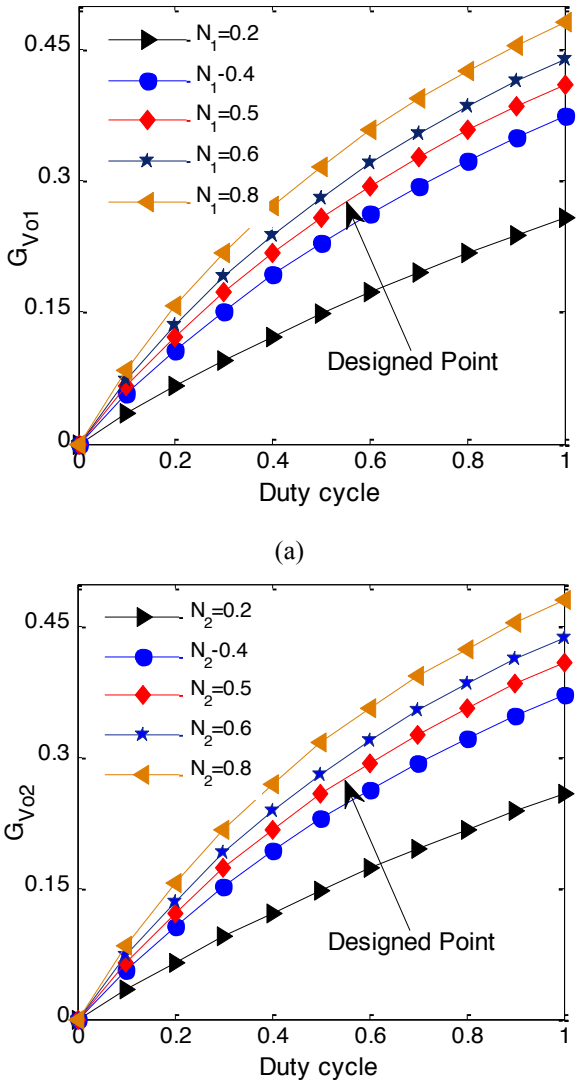


Fig. 5 (a) Voltage gain G_{Vo1} versus duty cycle (δ) for different N_1; (b) Voltage gain G_{Vo2} versus duty cycle (δ) for different N_2.

$$L_{LS1(\min)} = \frac{\left(v_{dc} - V_{o1}\right)N_1\delta}{2I_{o1}\left(1+N_1\right)f_s}$$
$$L_{LS2(\min)} = \frac{\left(v_{dc} - V_{o2}\right)N_2\delta}{2I_{o2}\left(1+N_2\right)f_s} \tag{25}$$

The required value of L_{S1} and L_{S2} for DCM should be selected such that $L_{S1} << L_{S1\ (min)}$, $L_{S2} << L_{S2\ (min)}$ and vice versa for CCM. The primary winding inductance L_{P1} and L_{P2} can be calculated by using the formula $N_1 = \sqrt{L_{S1}/L_{P1}}$ and $N_2 = \sqrt{L_{S2}/L_{P2}}$ respectively. The C_{o1} and C_{o2} [14] must be selected sufficient value to provide allowable output voltage ripple and to supply the load continuously.

$$C_{o1} \geq i_{o1}/2\omega\Delta V_{co1}$$
$$C_{o2} \geq i_{o2}/2\omega\Delta V_{co2} \quad (26)$$

Where, ΔV_{co1} and ΔV_{co2} are output ripple voltage of load-1 and load-2 respectively, $\omega=2\pi f_l$= angular frequency. In OSDO-CIB converter, the voltage stress of switch can be predicted by the peak value of the rectified voltage plus primary winding voltage. In a similar way the voltage stress of freewheeling diodes (D_1 & D_2) can be predicted by secondary winding voltage plus output voltage.

$$v_{ds} = v_{dc} + v_{LP1}, \quad \text{where } v_{LP1} = v_{LP2} = v_{LP} \quad (27)$$

$$v_{d1} = v_{LS1} + V_{o1} = N_1 v_{LP1} + V_{o1} \quad (28)$$

$$v_{d2} = v_{LS2} + V_{o2} = N_2 v_{LP2} + V_{o2} \quad (29)$$

3. Implementation and Result Analysis

In order to verify the feasibility of PFC-based OSDO-CIB converter, an experimental prototype circuit as shown in Fig. 6 has been built and tested practically. For experimental validations, the range of 90-130V input voltage and source frequency of 50 Hz are considered. However, the input voltage can be extended for universal range also. The specifications, design parameters and key components of proposed converter are described in Table I. The switching frequency (f_s) of 50 kHz are selected; accordingly, CIs T_1 and T_2 are prepared with ferrite core (EE 36/18/11). The L_{P1} (L_{P2}) of T_1 (T_2) is made of 14 turns (SWG 19) to accomplish required inductance value of 171µH. The L_{S1} (L_{S2}) of T_1 (T_2) is made of 7 turns (SWG 19 and SWG 18, parallel twisted wires) to accomplish required inductance value of 46 µH. The low-cost PWM IC TL494 is used to generate the 50 kHz switching pulse with suitable values of timing resistor (R_T) and capacitor (C_T). A low-cost driver IC IR2110 is used to drive the switching device of the converter.

Fig. 7 to Fig. 9 illustrates the experimental waveform of ac source voltage (V_s), ac source current (I_s), FFT waveform of source current, switch voltage (v_{ds}), diode voltage (v_{D1}), coupled inductor currents (i_{LP1}, i_{LS1}, i_{LP2} & i_{LS2}) and coupled inductor voltages (v_{LP1}, v_{LP2}, v_{LS1} & v_{LS2}) for various source voltage of 90 V, 110 V and 130 V respectively. From Fig. 7(a), it can be noticed that line current is nearly sinusoidal and in-phase with voltage while maintaining good PF. Generally, in low power level controlling the PF is difficult because of a significant decrease in source current magnitude at a higher value of ac input voltage. However, proposed PFC-based OSDO-CIB converter can achieve high PF in the range of 0.975-0.979 (say near unity) and %THD is nearly 15.64% (even less) over an input voltage range of 90-130V. As shown in Fig. 7-Fig. 9, the waveform of i_{Ls1} and i_{Ls2} evident that the desired DCM operation of proposed converter. It can be observed from Fig. 7(c) that the switch S voltage exhibit voltage spikes at turn-off instant which leads to a slight increase in voltage rating of the switching device. However, it is not much significant as compared with the reduction in on-state switch current (i_s) and off-state diode voltages (v_{D1}, v_{D2}).

Table 1 *Specifications and design Parameters*

Parameter description		Value / model no.
Source voltage (V_s),		90 -130 V_{rms}
Supply frequency (f_l)		50 Hz
Rectifier diodes		MUR 160 (4)
MOSFET (S)		IRF 740
Diodes (D_1,D_2)		STTH8L06FP (2)
Switching Frequency (f_s)		50 KHz
Coupled Inductor	T_1	L_{P1}=171.3µH, L_{S1}= 46.2µH
	T_2	L_{P2}=171.8µH, L_{S2}= 45.7µH
capacitor (C_{o1}, C_{o2})		2 x 1500µF/50 V

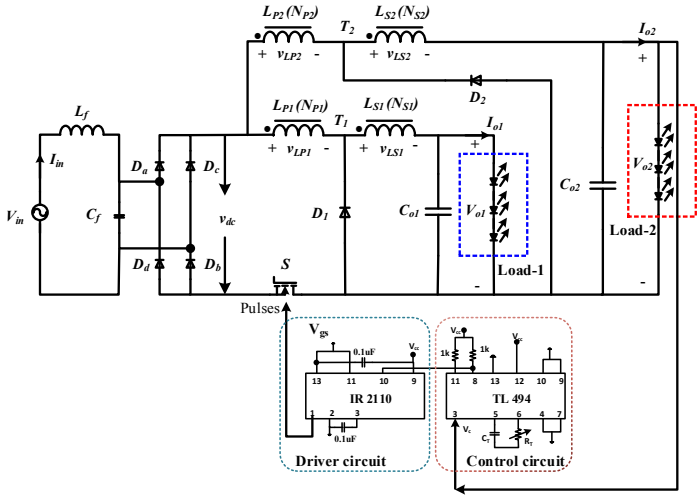


Fig. 6 Implementation of PFC-based OSDO-CIB converter with TL 494

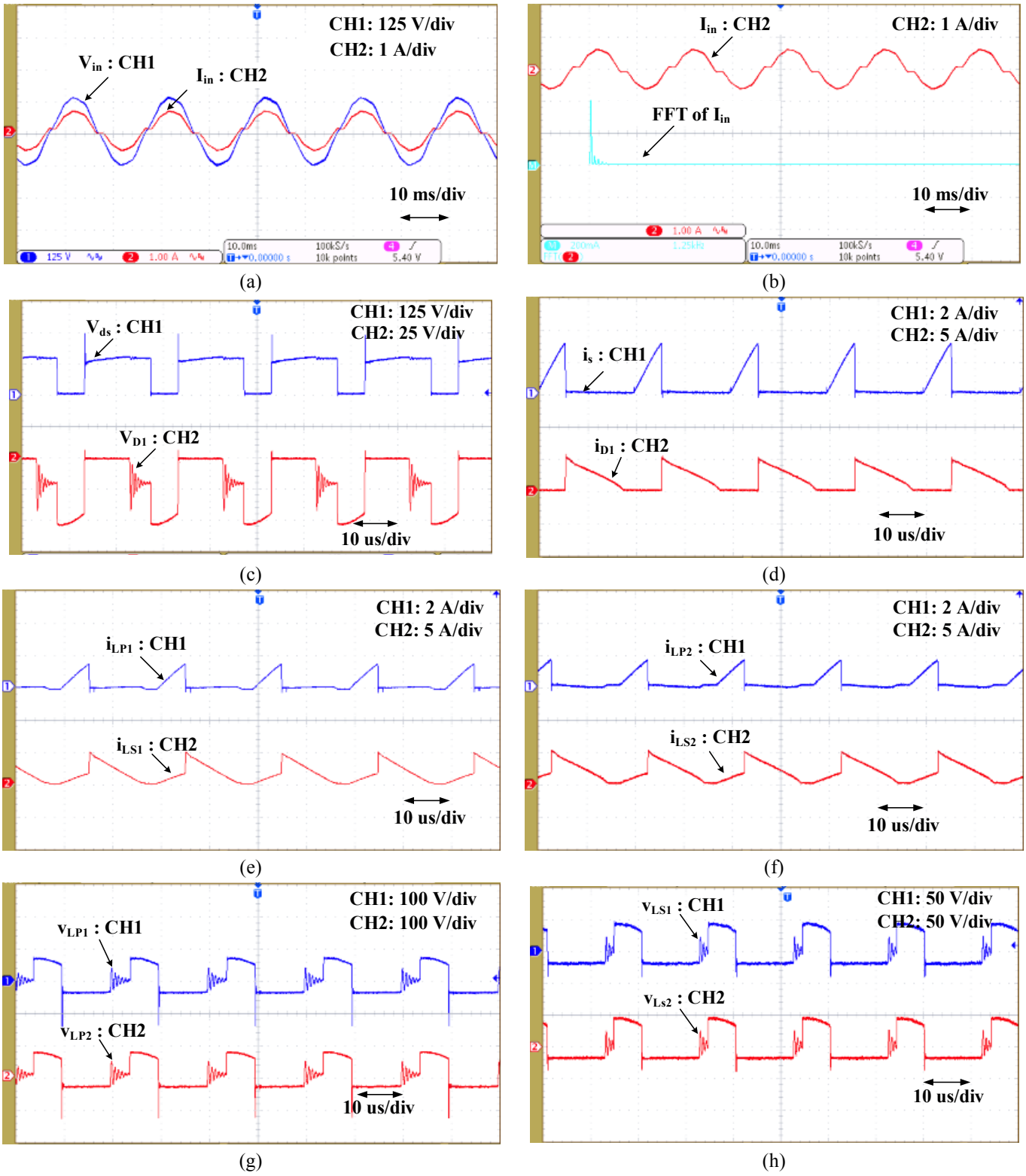


Fig.7. Experimental Waveforms at V_{rms}=90 V; **(a)** source voltage (V_{in}) and source current (I_{in}); **(b)** source current and FFT of I_{in}; **(c)** switch voltage (v_{ds}) and diode voltage (v_{D1}); **(d)** switch current (i_s) and diode current (i_{D1}); **(e)** CI (T_1) currents (i_{LP1}, i_{LS1}); **(f)** CI (T_2) currents (i_{LP2}, i_{LS2}); **(g)** primary winding voltage of coupled inductors T_1 and T_2 (v_{LP1}, v_{Lp2}); **(h)** secondary winding voltage of coupled inductors T_1 and T_2 (v_{LS1}, v_{LS2}).

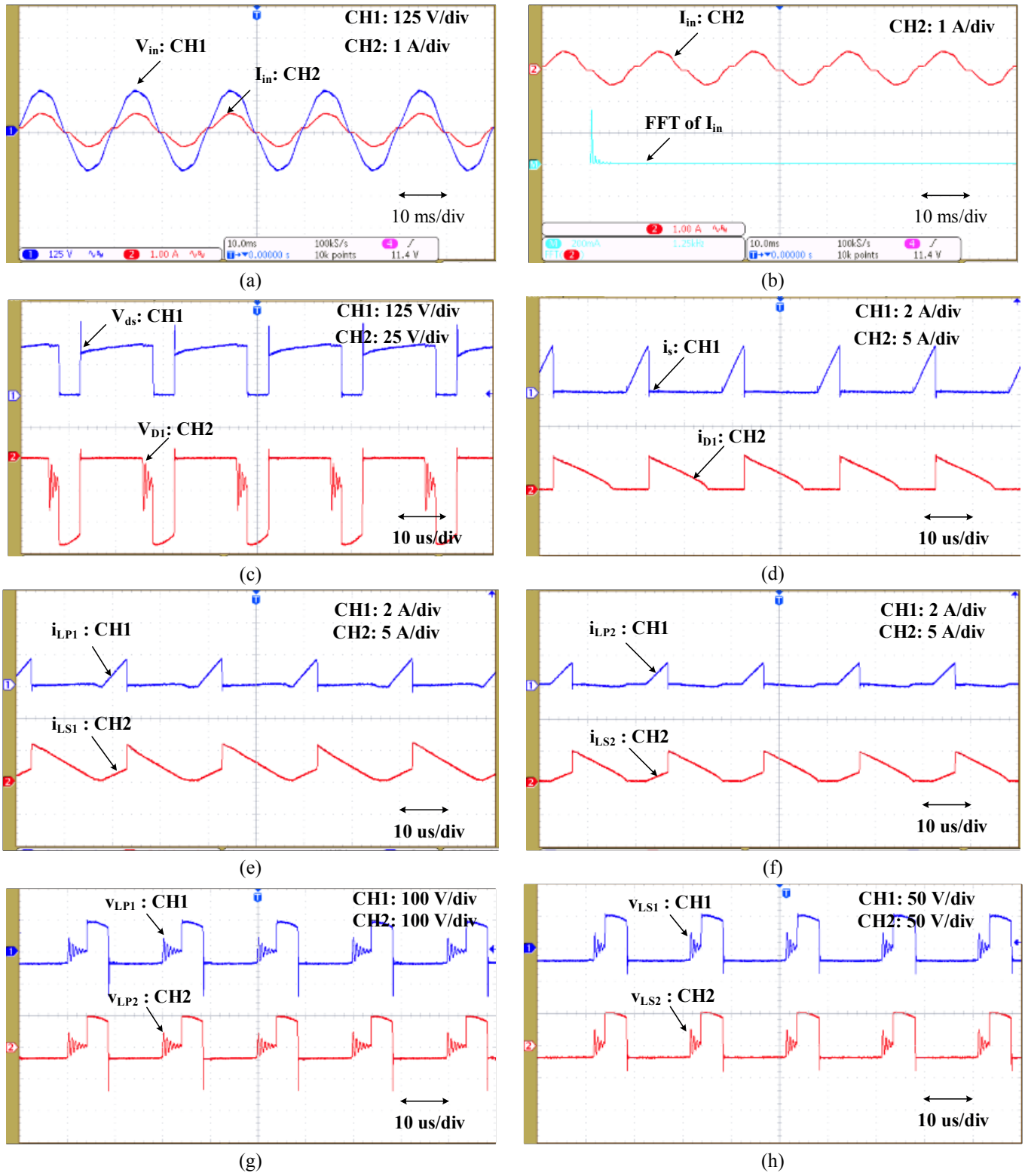


Fig.8. Experimental Waveforms at V_{rms}=110 V; **(a)** source voltage (V_{in}) and source current (I_{in}); **(b)** source current and FFT of I_{in}; **(c)** switch voltage (v_{ds}) and diode voltage (v_{D1}); **(d)** switch current (i_s) and diode current (i_{D1}); **(e)** CI (T_1) currents (i_{LP1}, i_{LS1}); **(f)** CI (T_2) currents (i_{LP2}, i_{LS2}); **(g)** primary winding voltage of coupled inductors T_1 and T_2 (v_{LP1}, v_{Lp2}); **(h)** secondary winding voltage of coupled inductors T_1 and T_2 (v_{LS1}, v_{LS2}).

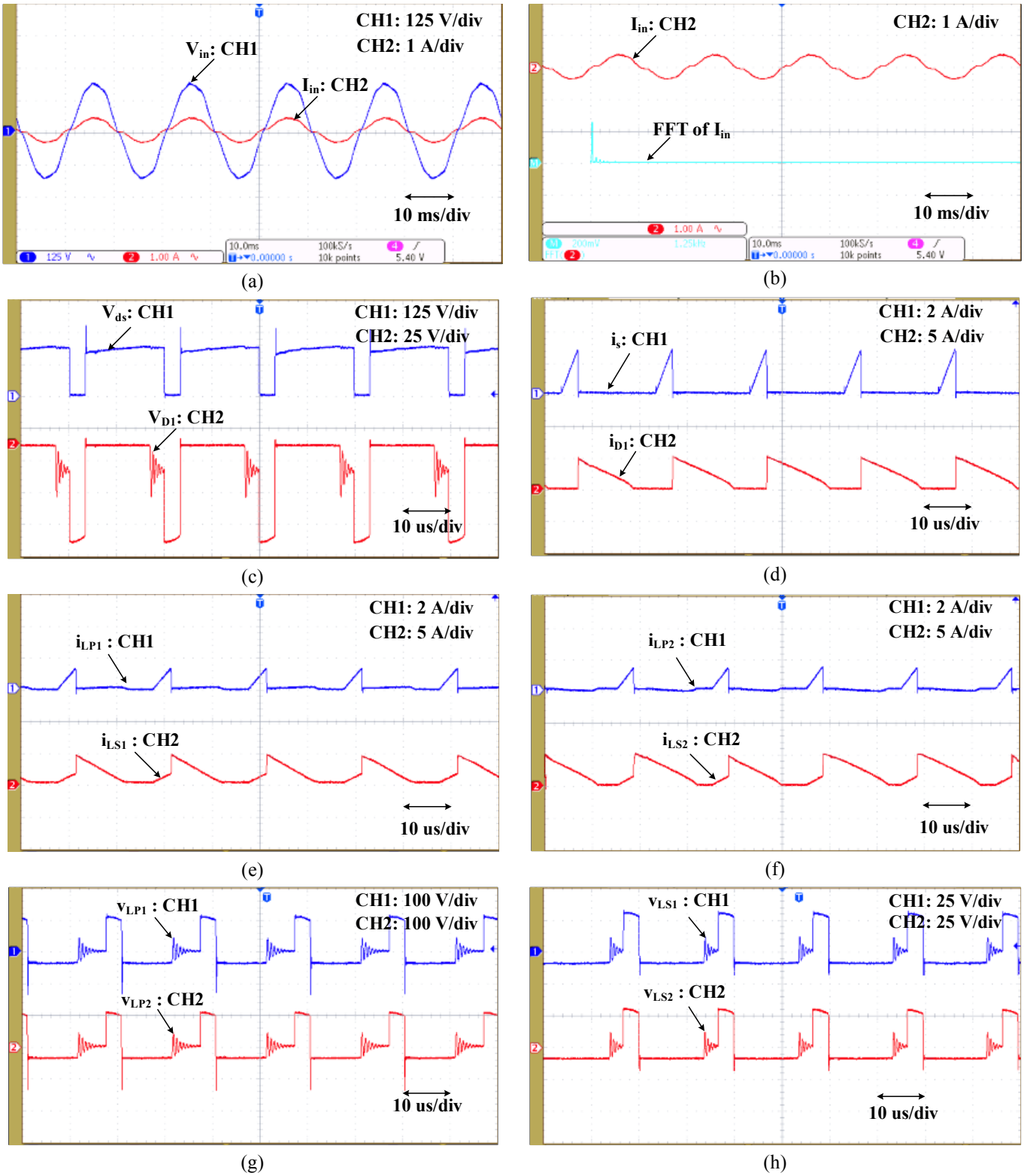
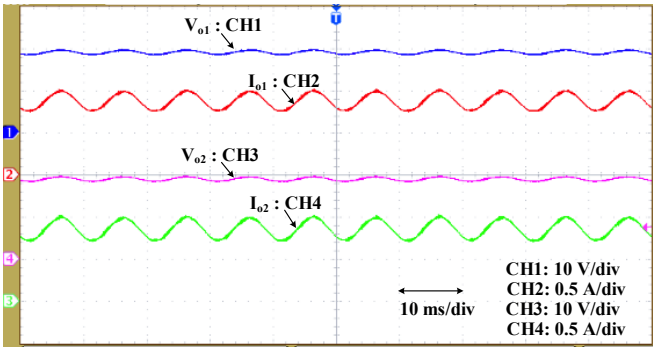
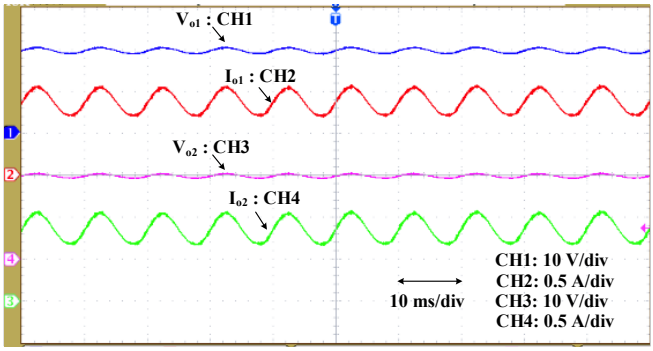


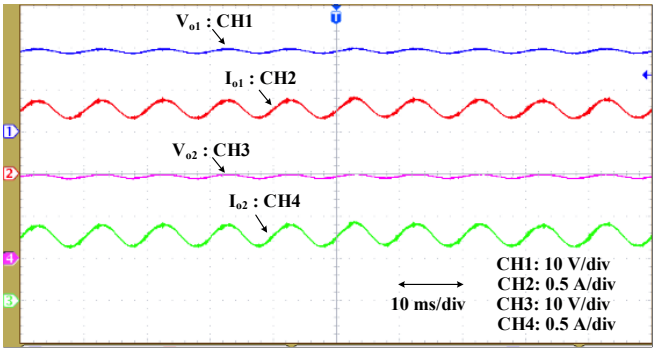
Fig.9. Experimental Waveforms at V_{rms}=130 Vrms; **(a)** source voltage (V_{in}) and source current (I_{in}); **(b)** source current and FFT of I_{in}; **(c)** switch voltage (v_{ds}) and diode voltage (v_{D1}); **(d)** switch current (i_s) and diode current (i_{D1}); **(e)** CI (T_1) currents (i_{LP1}, i_{LS1}); **(f)** CI (T_2) currents (i_{LP2}, i_{LS2}); **(g)** primary winding voltage of coupled inductors T_1 and T_2 (v_{LP1}, v_{Lp2}); **(h)** secondary winding voltage of coupled inductors T_1 and T_2 (v_{LS1}, v_{LS2}).



(a)



(b)



(c)

Fig.10. Experimental waveforms of output voltage and current of load-1 and load-2; **(a)** V_{rms}=90V;**(b)** V_{rms}=110V; **(c)** V_{rms}=130V.

Fig. 10 shows the experimental waveforms of output voltages (V_{o1} & V_{o2}) and output currents (I_{o1} & I_{o2}) at various ac input voltages of 90V, 110V and 130V respectively. From Fig. 10 (a)-(c), it is evident that the output voltages of load-1(V_{o1}) and load-2 (V_{o2}) are maintaining near desired value of 19.5 V with appropriate selection of duty cycle (δ) with various source voltages.

Fig. 11 depicts the comparison of measured efficiency of proposed OSDO-CIB converter with conventional buck converter. From Fig. 11 it confirms that the efficiency of proposed converter is above 89% at full load conditions over an input voltage range of 90-130V. In comparison with conventional single output buck converter the proposed OSDO-CIB converter achieved 5% more efficiency. The measured results of current harmonics are shown in Fig. 12(a), which convey that OSDO-CIB converter can meet the IEC 61000-3-2 class C standards. The measured THD is 15.64% at an input voltage of 110V. Fig. 12(b) demonstrates the measured power factor over an input voltage range of 90-130V. From Fig. 12(b) it can be observed that the PF is obtained to be 0.979.

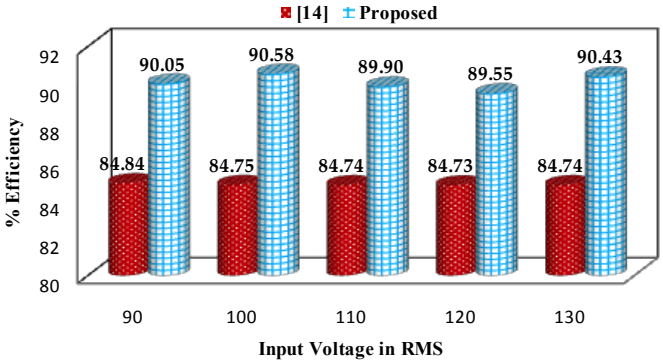
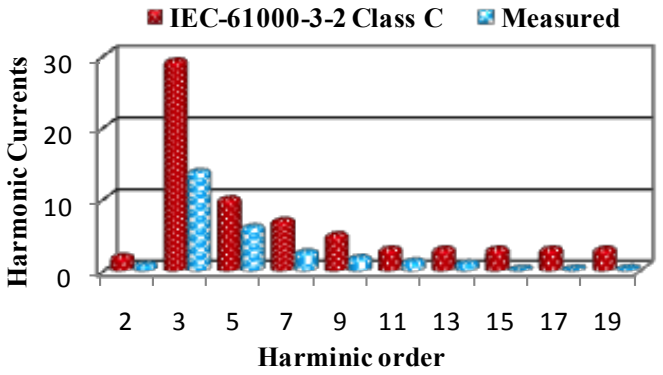
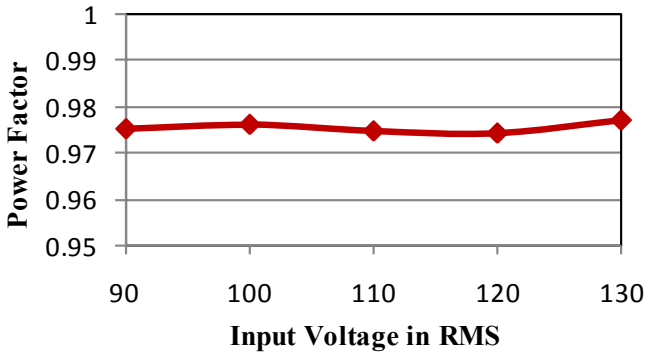


Fig. 11 Measured Efficiency with a variation of input RMS voltage.



(a)



(b)

Fig.12 (a) Measured results of current harmonics; **(b)** Measured power factor with a variation of the input voltage.

A comparison of proposed PFC-based OSDO-CIB converter with other types of single stage PFC topologies is to drive the multi-loads and also, it can be extended to any number of loads. In addition, OSDO-CIB utilizes CIs instead of using two separate inductors that result in several advantages such as, provide high step-down conversion, summarized in Table II. It can be noticed from Table II that the proposed OSDO-CIB converter requires only one switch reduction in device ratings, compact size, cost-effective and increases the overall converter efficiency. Thus, the proposed OSDO-CIB converter would be an ideal choice for multi-load applications.

TABLE II Comparative study

	[7]	[8]	[14]	[20]	[23]	Proposed
Mosfets	1	1	1	2	2	1
Fast Diodes	4	2	1	2	4	2
Slow Diodes	4	4	4	0	0	4
Inductors	1	2	3	1	0	1
CI	1	1	0	0	1	2
Capacitors	2	4	2	2	4	3
Input Voltage (V)	110	110	110	5	110	110
Output power (W)	70	8	13	1.56	100	34
Efficiency (%)	79.1	85.8	84.7	-	93.5	89.5
Output ports	1	1	1	2	2	2

4. Conclusions

This work proposes PFC-based OSDO-CIB converter, which can deal with a wide-range of ac source voltage to power multi-loads. This OSDO-CIB converter needs only one switch to feed multi-loads, thereby decreases the component count, reduces the switching losses and improves the efficiency. The OSDO-CIB converter utilizes CIs instead of using two separate inductors, which results in several advantages such as; provide wide-range step-down conversion, reduction in device ratings, effective utility of magnetic core, compact size, cost-effective and increased efficiency. The PFC-based OSDO-CIB converter operating in DCM provides a high PF, and low THD. A prototype of proposed LED driver with a power rating of 34 W (two loads of 17 W each) has been built and tested in the laboratory. The experimental validation and extensive result analysis have been made, which clearly shows an advantage of PFC-based OSDO-CIB LED driver. For ac input voltage range of 90-130V, the PF is obtained to be 0.979, measured efficiency is above 89.55% and THD is 15.64% at rated load conditions. Thus, this PFC-based OSDO-CIB converter would be an ideal choice for multi-load applications.

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