Coupled Inductor Based Soft Switched Interleaved DC-DC Converter for PV Applications

Sheshidhar Reddy Addula *, M.Prabhakar**‡

*M.Tech Student, School of Electrical Engineering, VIT University, Chennai, Vandalur-Kelambakkam Road, Chennai – 600127.

**Associate Professor, School of Electrical Engineering, VIT University, Chennai, Vandalur-Kelambakkam Road, Chennai – 600127.

(sheshi013@gmail.com, prabhakar.m@vit.ac.in)

‡ Corresponding Author; M.Prabhakar, Associate Professor, School of Electrical Engineering, VIT University, Chennai, Vandalur-Kelambakkam Road, Chennai – 600127. Tel: +91 44 3993 1154, Fax: +91 44 3993 2555, prabhakar.m@vit.ac.in

Received: 16.01.2016 Accepted: 05.02.2016

Abstract- Interleaved DC-DC converter topologies are gaining popularity for their use as an interface between photovoltaic (PV) source and load. In this paper, a family of coupled inductor (CI) based novel soft switched interleaved DC-DC converter topologies has been proposed to be used for PV application. The topology has been developed from the interleaved stage so as to reduce the input current ripple. The CI stage has been introduced to enhance the power handling capability of the converter. In addition, diode-capacitor multiplier (DCM) cells are connected to obtain higher voltage gain. Since voltage gain extension is obtained through DCM cells and the turns-ratio of the CI, the voltage stress on the main power switches is only a fraction of the output voltage. Further, the diodes present in each DCM cell need to withstand only a low reverse voltage. To enhance the operating power conversion efficiency, the power switches are turned ON under zero voltage switching (ZVS) condition. Experimental results obtained from a 20V-360V, 200W prototype converter validate the operating principle and the advantageous features of the developed topology.

Keywords- Coupling circuits; DC-DC power conversion; power converter; resonant power conversion; voltage multipliers.

1. Introduction

The quantum of electric power generated from renewable energy sources like solar and fuel cells is consistently increasing over the past decade [1]-[5]. As the output voltage levels from these sources are relatively low, these voltages must be stepped up considerably before practical utilization. Hence, there is a need to use a high step up DC-DC converter. Conventional boost converter cannot provide high voltage gain due to reverse recovery problem of output diode and higher power losses when operated at higher duty ratios. Due to these practical limitations of a classical boost converter, several novel topologies which are capable of providing high voltage gain without suffering from similar problems were developed [6]-[8].

Some CI based topologies were developed to improve the voltage gain and power handling capability of the converters [9]-[12]. Nevertheless, some topologies operated under discontinuous conduction mode (DCM) and eventually degraded the system performance. Few transformer based topologies were experimented for obtaining higher voltage conversion ratio [13] and [14]. However, such topologies cannot be operated at high frequencies due to increment in (a) the transformer losses, (b) probability of core getting saturated and (c) overall cost and weight of the system. Moreover, leakage inductance of the transformer winding causes electromagnetic interference (EMI) and results in undesirable voltage and current spikes appearing across the switch.

To overcome these drawbacks, transformerless topologies were presented in [15] and [16]. However, the voltage gain was limited and the switch suffered from higher voltage stress in these converters. Topologies based on voltage multiplier cells (VMCs) and multilevel converters (MLCs) were reported in [17] and [18] respectively. By using several VMCs or levels in MLCs, though higher conversion ratio can be achieved, component count increases. Moreover, beyond certain number of cells, these converters cannot deliver large power.

For PV fed applications, higher input current ripple leads to reduced life of the system. Interleaved converters

were proposed to alleviate the problem of higher input current ripple. Further, gain extension techniques were also implemented to take care of the voltage conversion ratio requirement. Interleaved converters with VMCs have been reported in [19] and [20]. To reduce the number of components used without compromising on voltage gain, interleaved converter with DCM cells have been developed and presented in [21]. This topology provides the same voltage gain with half the number of components used in VMC. However, the hard switching mechanism reduces the overall efficiency especially at higher power levels and switching frequencies. Some soft switched topologies that provide relatively large voltage gain at better efficiency are discussed in [22]-[27].

In this paper, a soft switched high gain DC-DC converter topology with reduced input current ripple and switch stresses with high power handling capability is presented. The paper is outlined as follows: section 2 presents the evolution of the proposed converter family while the developed converter is analysed using the operating modes and characteristic waveforms in section 3. In section 4, design details pertaining to various parameters like voltage gain, device stresses and soft-switching phenomena is presented. Experimental results and discussions are provided in section 5 while the conclusion is detailed in section 6.

2. Evolution of CI based DC-DC Converter Family

A two phase interleaved boost converter (IBC) is considered as the fundamental topology. Fig.1 (a) represents a CI based interleaved topology in which one of the phases of conventional IBC is left unchanged while the boost inductor is replaced by a CI in the other phase. Resultantly, the primary inductance of the CI acts as the energy storage and energy transfer inductor. The secondary of this CI is suitably connected to output capacitor (C02 in this case). The net output voltage is obtained across the series combination of output capacitors C01 and C02. Thus, the overall voltage gain contribution is due to two stages – the interleaved boost stage and the CI stage. By intuition, it can be realized that the overall voltage gain of this converter shall be higher than the conventional IBC due to CI with a turns ratio more than 1.

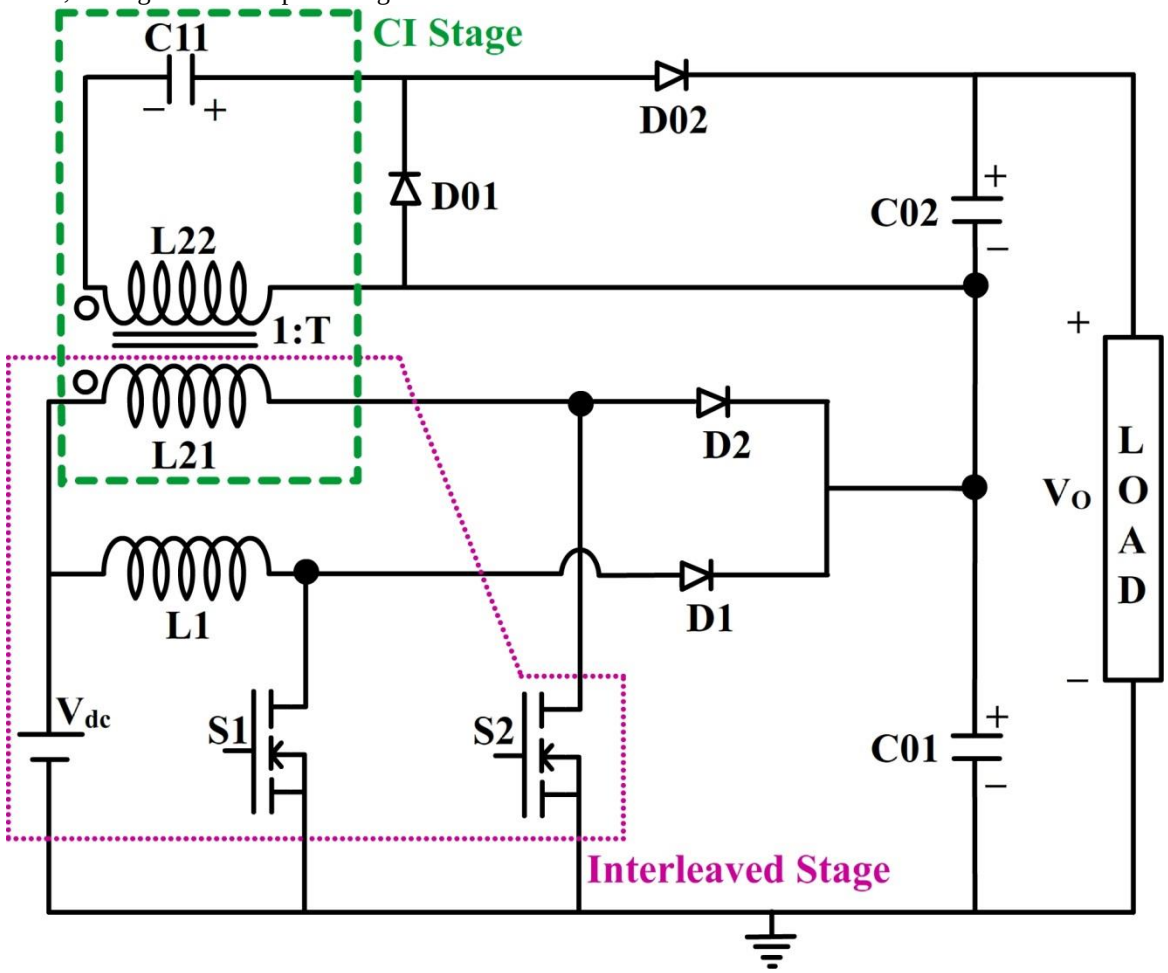

Fig.1 (a). Power circuit of CI based IBC.

To enhance the voltage gain and power handling capability, DCMs are judiciously added to CI based topology as shown in Fig.1 (b). Now, the three stages present are recognized as (i) interleaved stage, (ii) DCM stage and (iii) CI stage. Each stage has its own prominent feature as listed below:

- Interleaved stage aids in reducing the input current ripple.
- DCM stage provides high voltage gain with reduces number of components compared to VMC stages, thereby reducing circuit complexity and voltage stress on the main switch.

- CI stage helps to enhance the voltage gain and handle higher power.

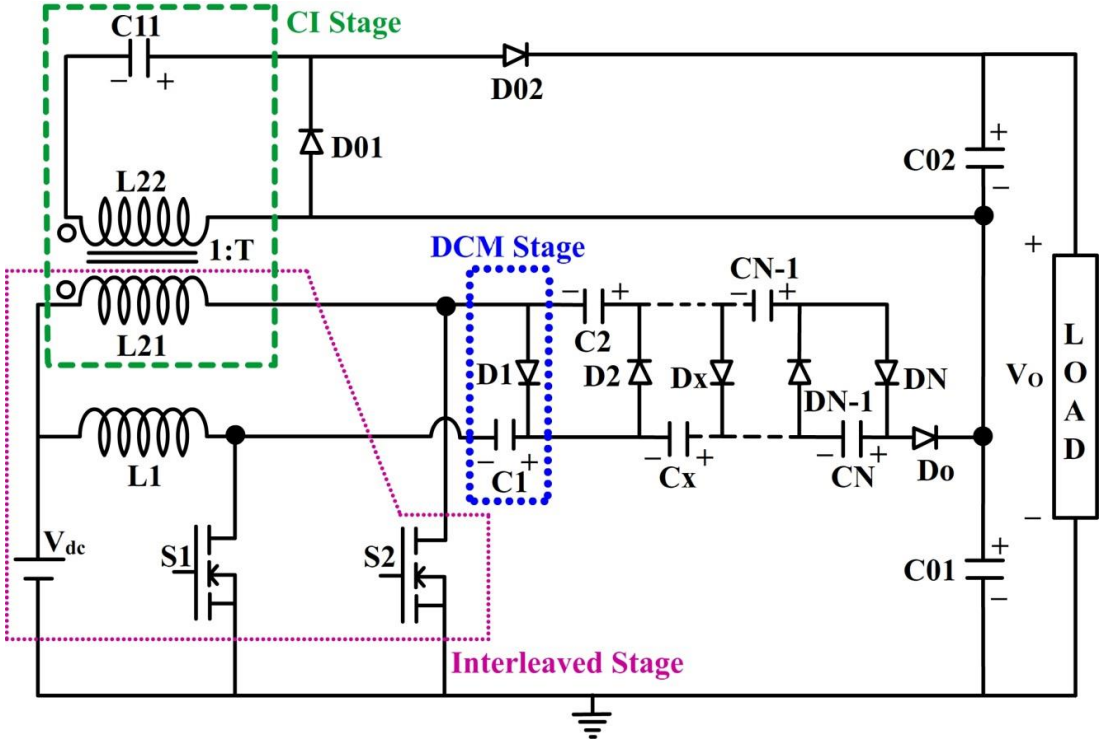

Fig.1 (b). Power circuit diagram of CI based IBC with N DCMs.

The voltage gain of the presented converter now depends on (i) turns-ratio of the CI (T) and (ii) number of DCMs used (N). This provides added flexibility to the user in terms of meeting the voltage gain requirement.

Extension of this concept leads to a generalized converter structure as depicted in Fig. 1(c). The converter structure has an interleaved converter with P phases using Q number of coupled inductors (Q ≤ P), each with T turns ratio. It must be noted that N number of DCM stages can also be added appropriately. The load is connected across the series combination of output capacitors.

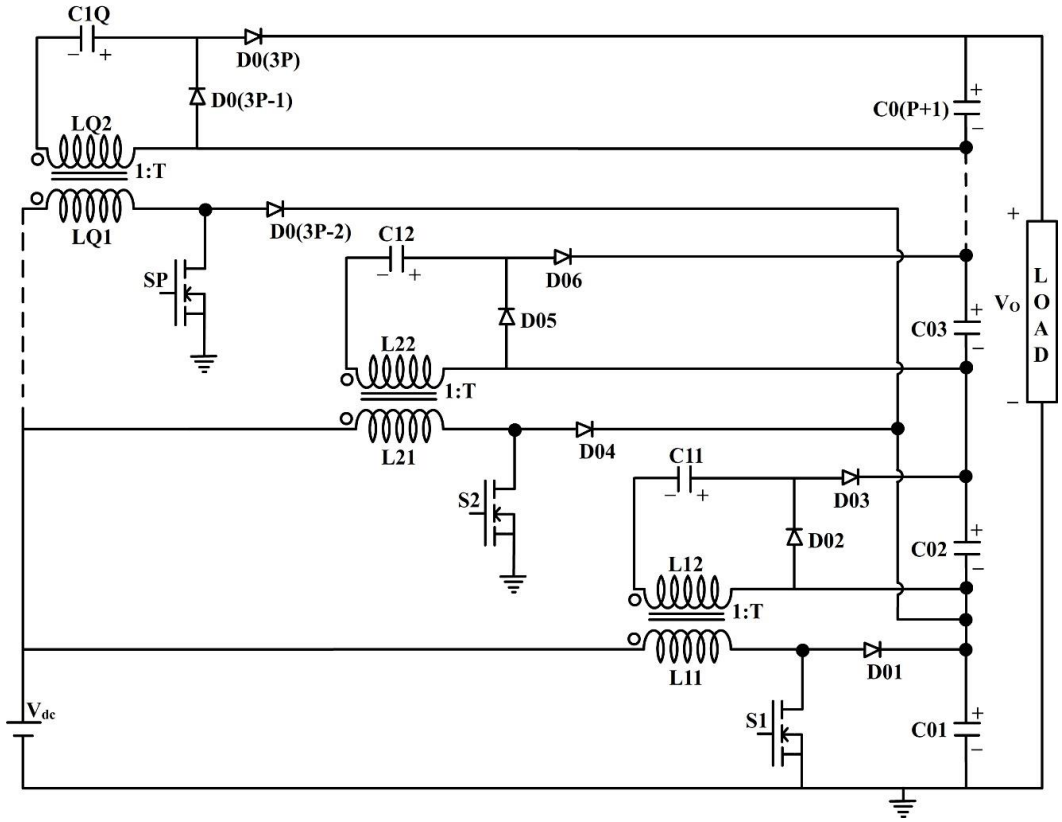

Fig.1 (c). Generalized structure of proposed coupled inductor based topology.

3. Analysis of Proposed Converter Topology

3.1. Power circuit

The proposed CI based soft-switched interleaved high gain DC-DC converter is shown in Fig.2. The circuit has two switches which are operated at 180° phase shift with a duty cycle of D. Diodes D_{S1} and D_{S2} are the intrinsic body diodes of S1 and S2 respectively. C_{S1} and C_{S2} are the resonating capacitors which have been added across the switches so as to undergo resonance with the inductors L1 and L21 in order to achieve ZVS turn ON of the switches. The diode-capacitor pair D1-C1 forms the 1st DCM cell. Similarly, the remaining DCM cells are obtained from D2-C2 through D5-C5. Diode D6 acts as the output diode while capacitors C01 and C02 serve as the output capacitors of CI and DCM stages. The load is connected across the series combination of output capacitors. Thus, a CI based soft-switched interleaved DC-DC converter containing 5 DCM cells is developed.

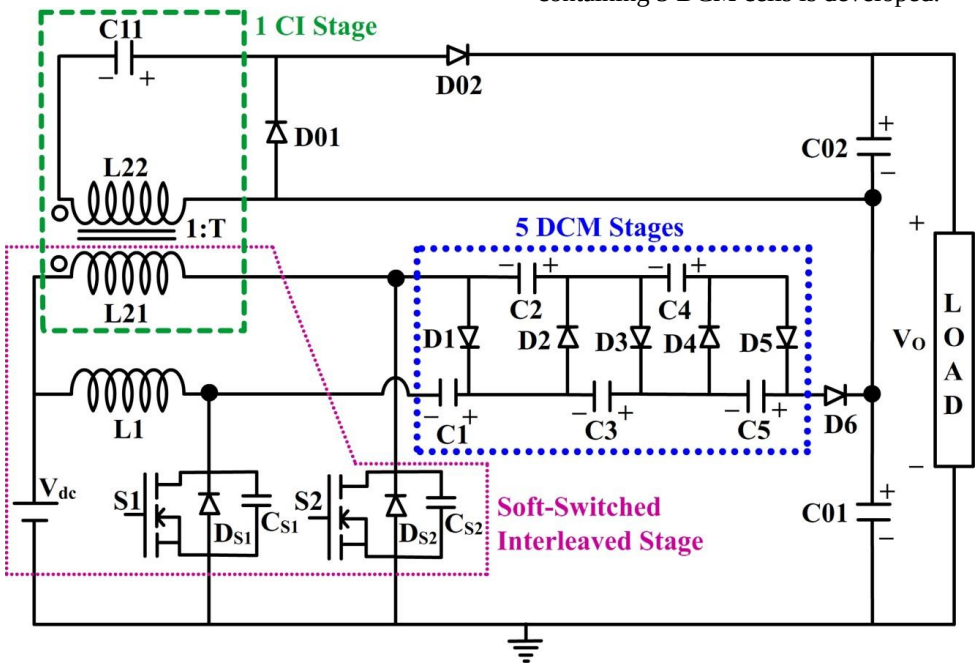

Fig.2. Power circuit diagram of the developed converter topology.

3.2. Modes of Operation

The operation of the proposed converter can be understood in six distinct modes. One switching cycle starts from t_0 and ends at t_6. Before the cycle starts, switch S2 is considered to be in conduction till t_0. The switches are operated at 0.5 duty ratio. The operating modes are explained as follows.

Mode 1($t_0 - t_1$): At t_0 gate pulse to switch S2 is removed. The resonant capacitor C_{S2} begins to charge towards the supply voltage. Current through the inductor L21 will be same as the charging current through resonant capacitor C_{S2}. As a result, voltage across C_{S2} increases gradually. Simultaneously, C_{S1} begins to discharge. As this is for shorter duration the polarity of induced voltage across secondary winding L22 does not change. The diode D02 will be conducting to charge output capacitor C02 of CI stage.

Mode 2($t_1 - t_2$): At time t_1, capacitor C_{S1} discharges completely and voltage across it becomes zero. The anti-body diode D_{S1} of switch S1 starts conducting due to induced voltage across L11. This results in small current flow through diode D_{S1}. Because the body diode conducts, the current through S1 will be negative for a short duration. Further, the voltage across switch S1 is clamped at zero. In DCM stage, as switch S2 turns OFF, the voltage across inductor L21 forward biases the diodes D1, D3 and D5 while in CI stage, the polarity of induced voltage across L22 changes. As a result, D01 starts to conduct and the stored energy in the inductor is transferred to the capacitor C11 while C02 discharges through the load.

Mode 3($t_2 - t_3$): At t_2, gate pulse to switch S1 is provided and S1 turns ON under ZVS condition. Now, S1 is ON and S2 is OFF. Diodes D1, D3 and D5 conduct while diodes D2, D4 and D6 remain reverse biased. Inductor current I_{L1} increases linearly whereas current through L21 (I_{L21}) decreases linearly. A part of I_{L21} flows through capacitors C2, C3, C4 and C5 in such a way that C2 and C4 discharge while capacitors C3 and C5 charge. Other part of I_{L21} flows through D1 to charge C1. Due to this current flow, the voltage across C1, C3, C5 increases while capacitor voltages V_{C2} and V_{C4} decrease. The operation of CI stage remains same as that of Mode 2. The output capacitors C01 and C02 discharge through the load. This mode ends at t_3.

Mode 4($t_3 - t_4$): At t_3, switch S2 is turned OFF. Therefore, a part of the energy stored in L1 is transferred to capacitor C_{S1}. The capacitor C_{S1} begins to charge while capacitor C_{S2} begins to discharge. As a result, voltage across C_{S1} raises while voltage across C_{S2} decreases gradually.

Mode 5($t_4 - t_5$): At time t_4, capacitor C_{S2} is completely discharged and voltage across it becomes zero. This clamps the voltage across switch S2 at zero. The anti-body diode D_{S2} begins to conduct and results in small negative current flow through the switch. At the DCM stage, as switch S1 turns OFF, the inductor L1 starts discharging through diodes D2, D4 and D6. With regards to the CI stage, the polarity of induced voltage across L22 gets

reversed due to inductive kickback. Consequently, D02 starts to conduct. Energy stored in the inductor L22 and capacitor C11 is transferred to the output capacitor C02. Thus, DCM stages charge capacitor C01 and output capacitor C02 charges in CI stage.

Mode 6($t_5 - t_6$): At time t_5, gate pulse to switch S2 is applied and S2 turns ON under ZVS condition. Thus, S2 is ON while S1 is OFF. Diodes D1, D3 and D5 are reverse biased while diodes D2, D4 and D6 will be conducting. Inductor current I_{L21} increases linearly whereas current through L1 (I_{L1}) decreases linearly. A part of I_{L1} flows through capacitors C1, C3 and C5 and discharges them while the remaining fraction of I_{L1} is used to charge capacitor C2, C4 through diodes D3 and D5 respectively. The operation of CI stage remains same as that of Mode 5. The output capacitors C01 and C02 will be charging and the sum of voltages appear across the load. The cycle ends at T_s. Figures 3(a) – 3(f) show the equivalent circuit during Mode 1 to Mode 6 while the characteristic waveforms are shown in Fig.4.

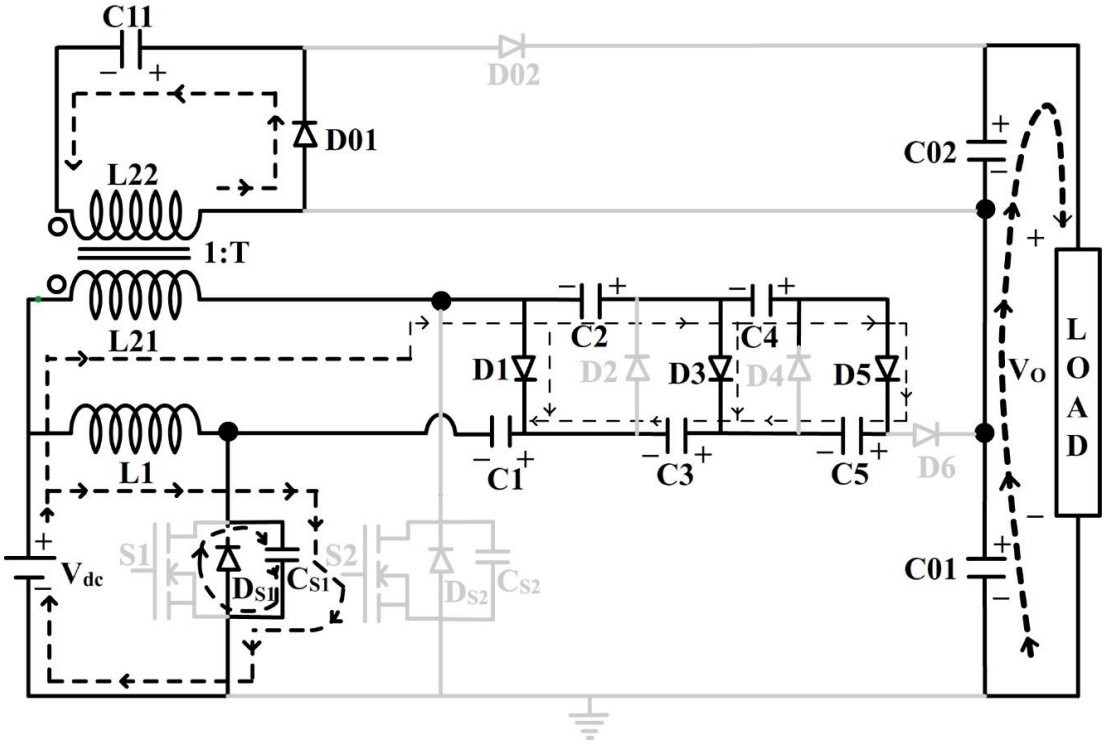

Fig.3 (a). Mode 1

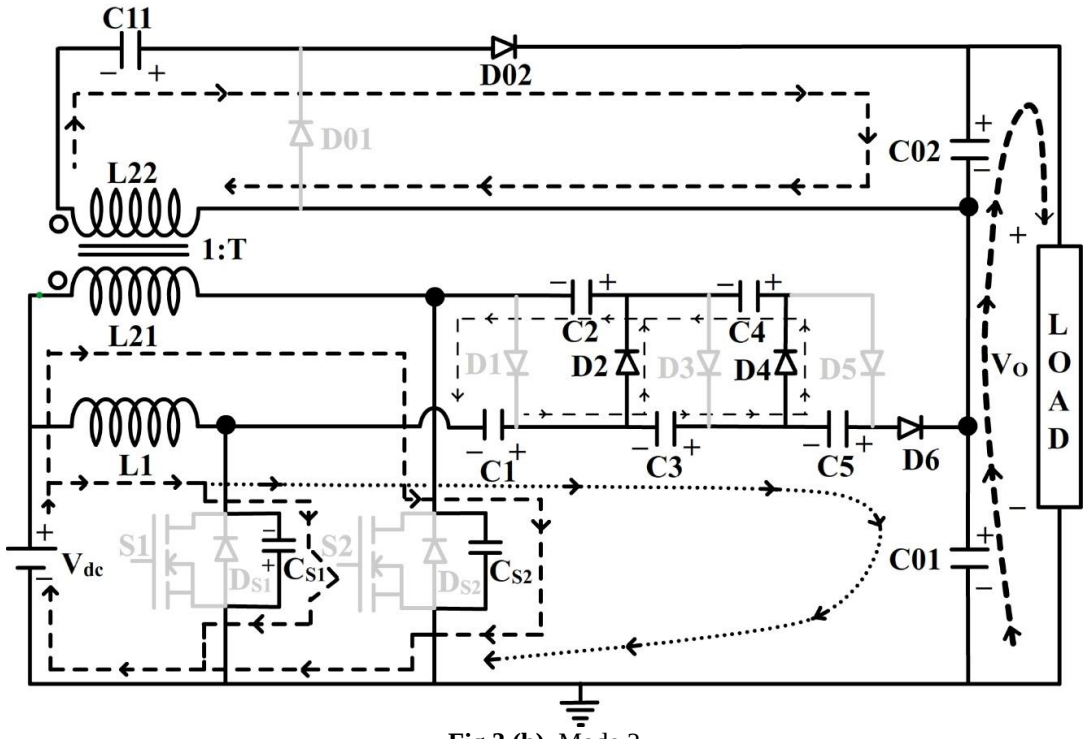

Fig.3 (b). Mode 2

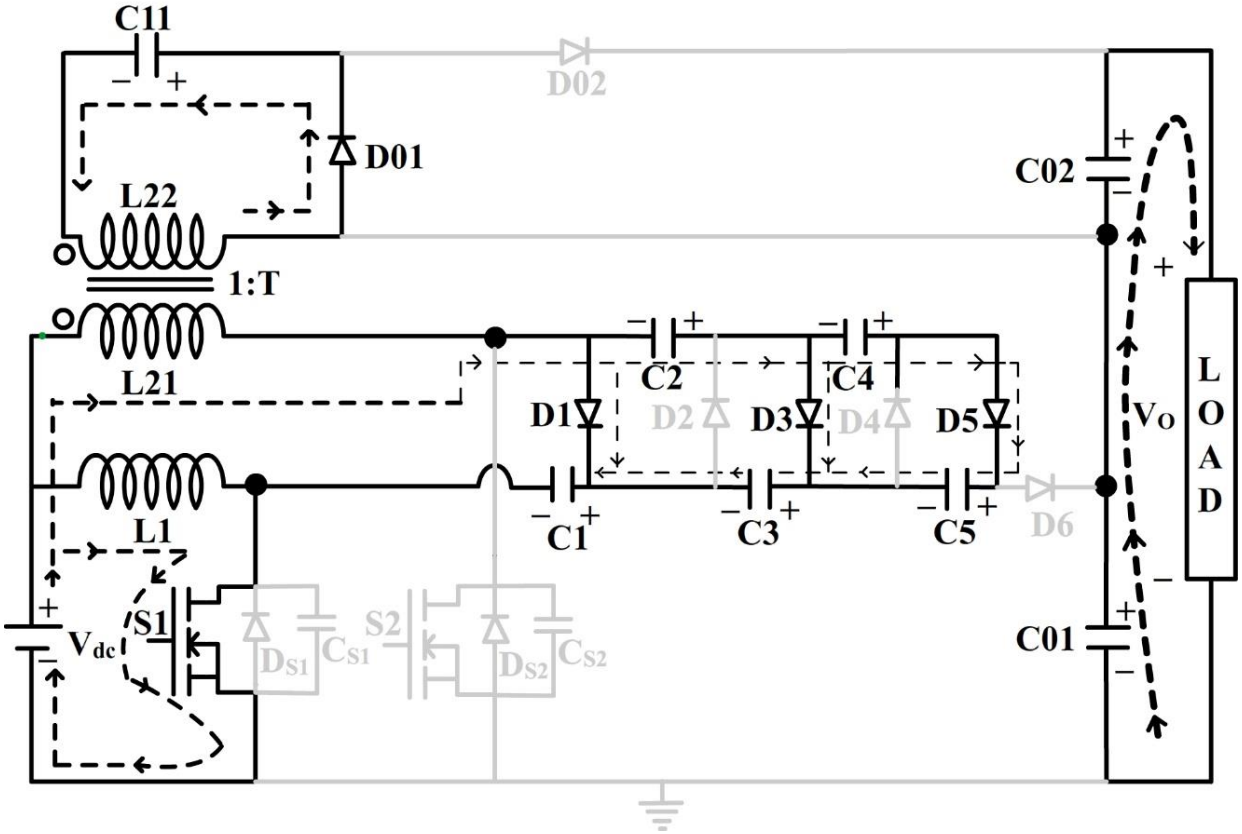

Fig.3 (c). Mode 3

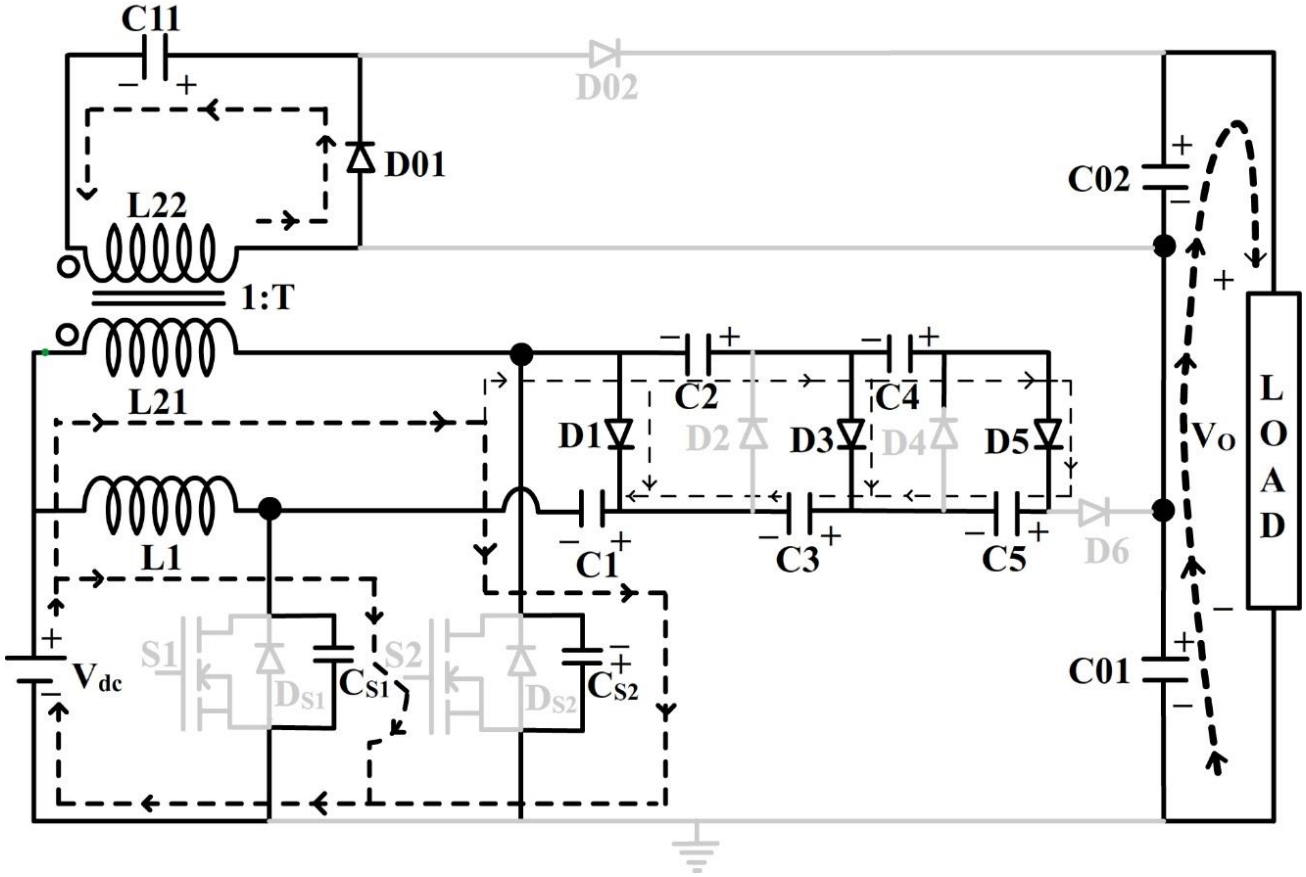

Fig. 3 (d). Mode 4

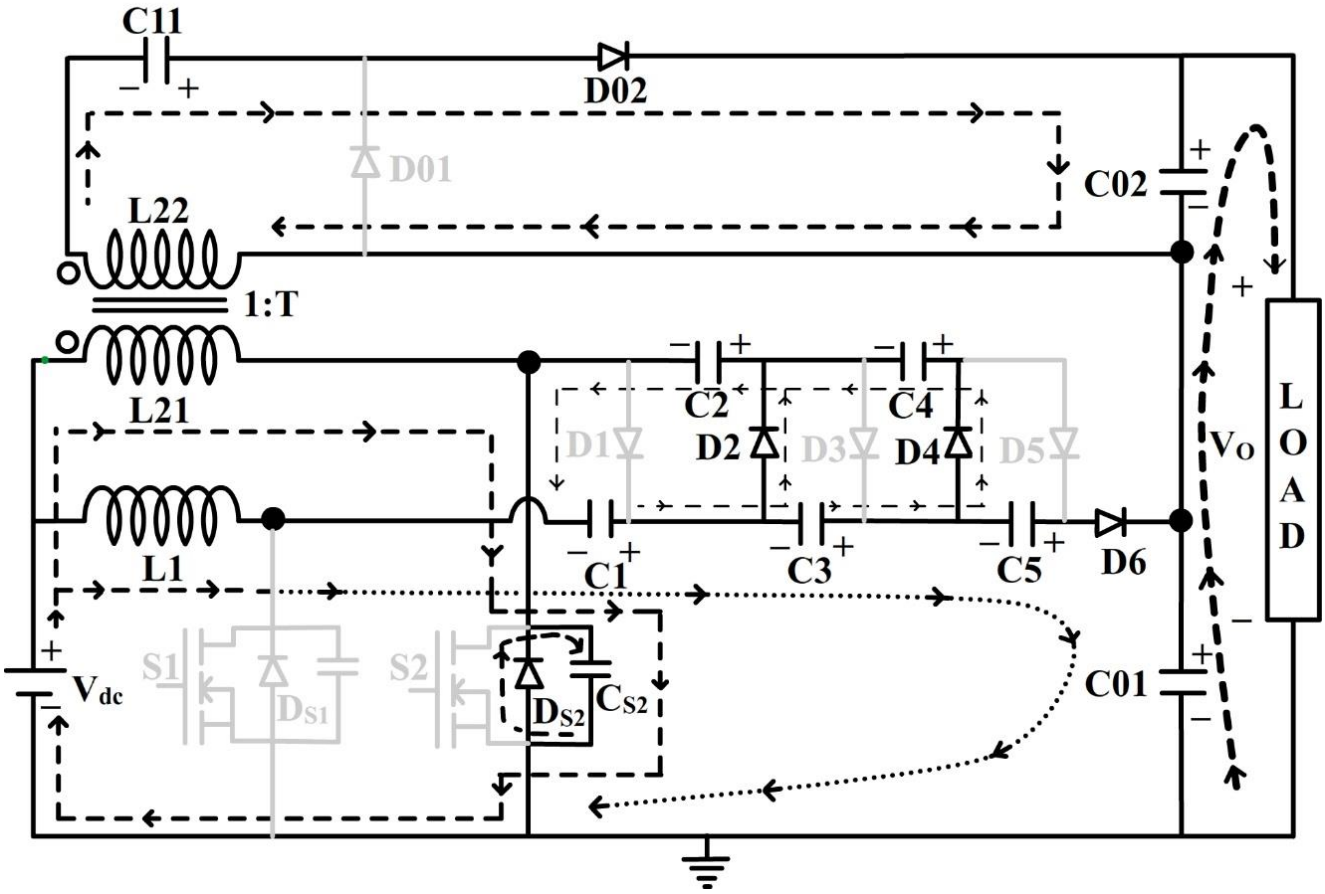

Fig. 3 (e). Mode 5

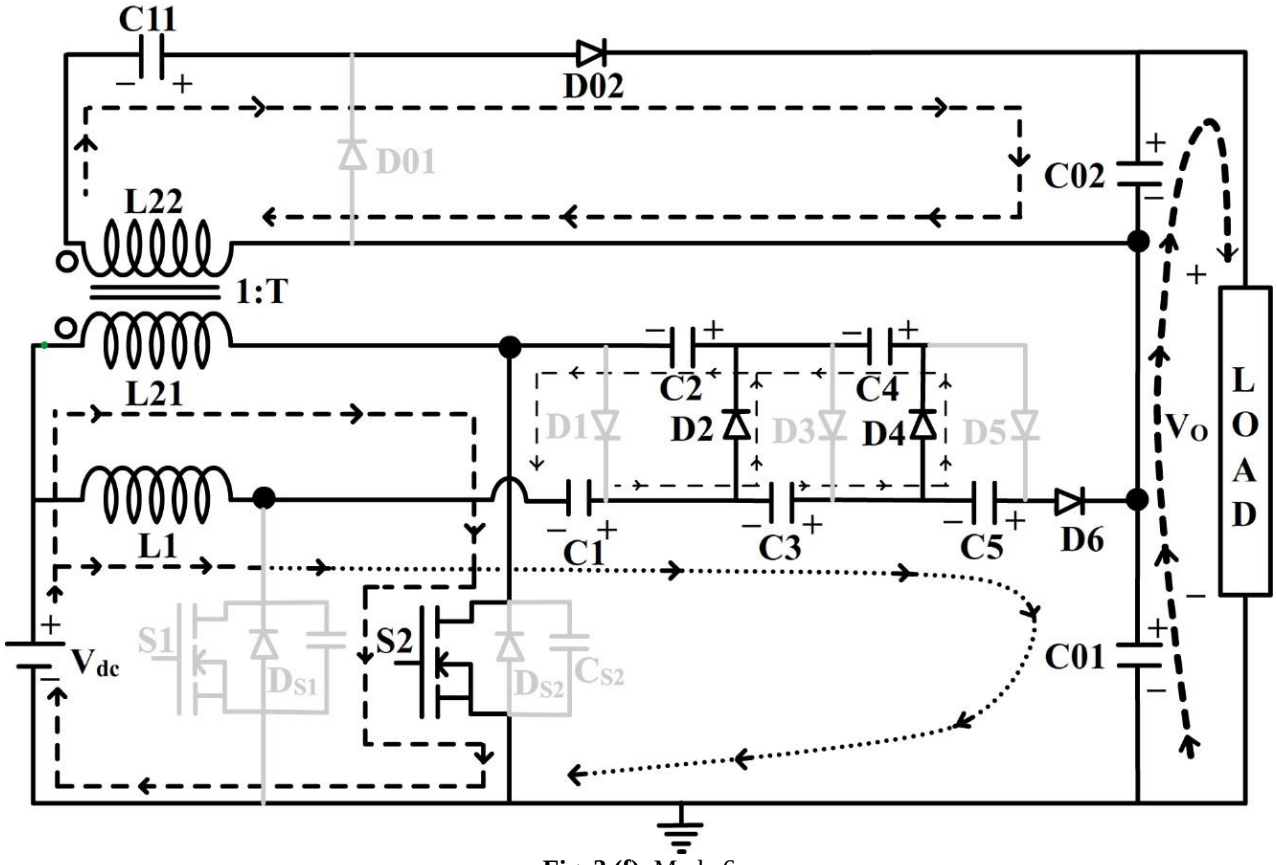

Fig. 3 (f). Mode 6

Fig.3. Equivalent circuit of the proposed converter during various operating modes.

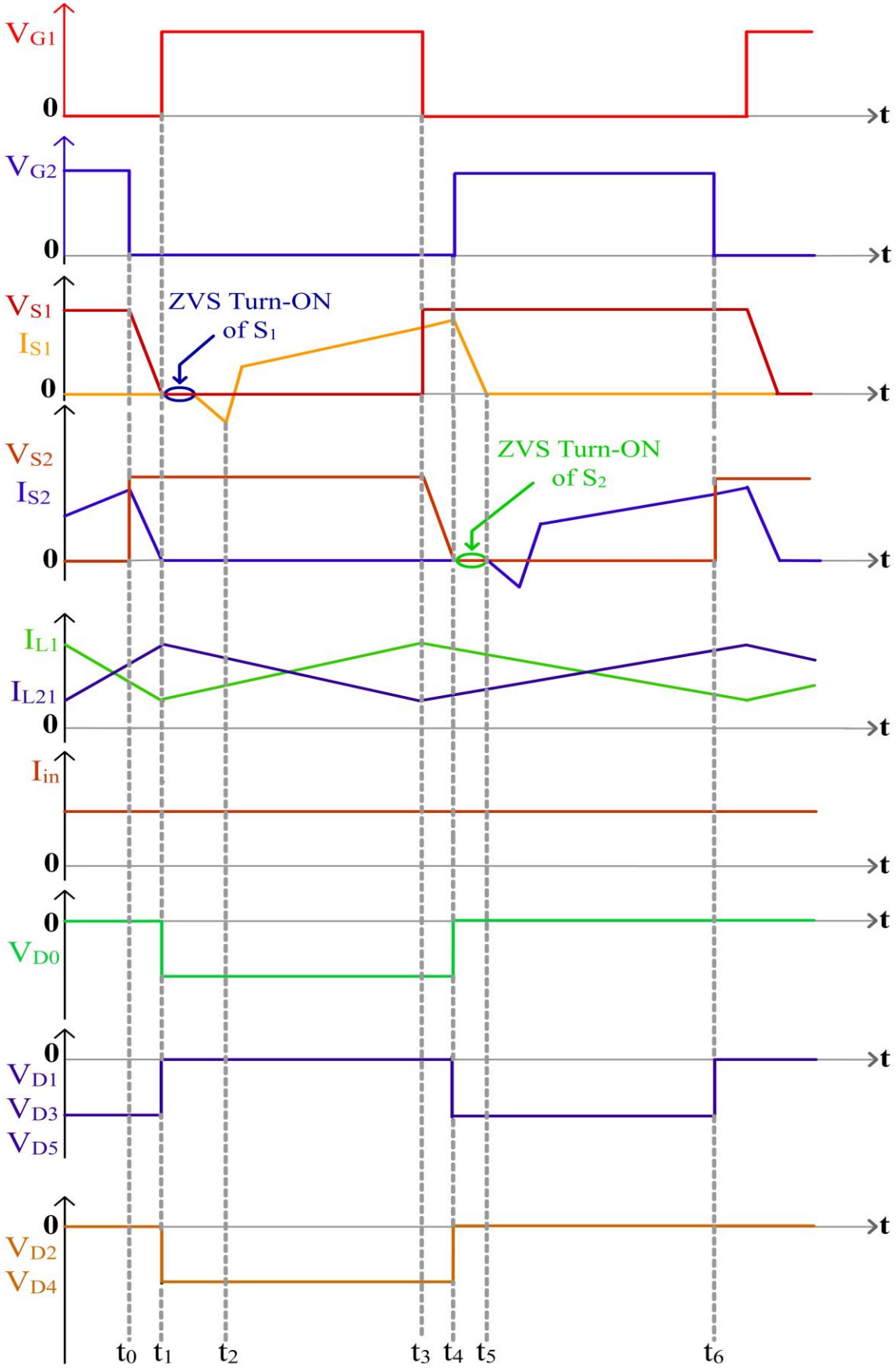

Fig.4. Characteristics waveforms of the proposed converter.

4. Design Details

4.1. Voltage gain

Voltage gain of the proposed converter depends on 3 stages. Since, the load is connected across the series combination of output capacitors C01 and C02, the overall voltage gain shall be expressed as

$$V_O = V_{C01} + V_{C02} \tag{1}$$

From Mode 3 (Fig. 5(c)), applying volt-second balance on inductors L1 and L21 gives,

$$V_{dc}D = (V_{C1} - V_{dc})(1-D) \tag{2}$$

By using equations (2)-(7), the voltages across capacitors are determined as

$$V_{C2} = V_{C3} = V_{C4} = V_{C5} = \frac{2V_{dc}}{1-D} \tag{8}$$

$$V_{C1} = \frac{V_{dc}}{1-D} \tag{9}$$

$$V_{C01} = \frac{6V_{dc}}{1-D} \tag{10}$$

Generally, for an identical topology with N DCM cells, the voltage across the DCM stage output capacitor is given by,

$$V_{C01} = \frac{(1+N)V_{dc}}{1-D} \tag{11}$$

For the CI stage, when switch S2 is ON, voltage across inductor L21 is given by

$$V_{L21} = V_{dc} \tag{12}$$

The voltage induced across the secondary winding will be turns ratio (T) times that of the primary voltage. Therefore,

$$V_{L22} = TV_{L21} = TV_{dc} \tag{13}$$

The voltage across CI stage output capacitor is given by

$$V_{C02} = V_{L22} + V_{C11} \tag{14}$$

When switch S2 is OFF, voltage across inductor L1 is obtained as

$$V_{L1} = \frac{DV_{dc}}{1-D} \tag{15}$$

The voltage across capacitor C11 is given by,

$$V_{C11} = TV_{L1} = \frac{TDV_{dc}}{1-D} \tag{16}$$

where T it the turns ratio of the CI.

Substituting equations (13) and (16) in equation (14) and simplifying, voltage across output capacitor C02 is derived as

$$V_{C02} = \frac{TV_{dc}}{1-D} \tag{17}$$

From equations (11) and (17), the expression for output voltage attainable from the proposed converter is derived as

$$V_{dc}D = (V_{C1} - V_{C2} + V_{C3} - V_{dc})(1-D) \tag{3}$$

$$V_{dc}D = (V_{C1} - V_{C2} + V_{C3} - V_{C4} + V_{C5} - V_{dc})(1-D) \tag{4}$$

where D is the duty ratio of the switches.

Applying volt-second balance on inductors L1 and L21 during Mode 6 (Fig. 3(f)) yields,

$$V_{dc}D = (V_{C2} - V_{C1} - V_{dc})(1-D) \tag{5}$$

$$V_{dc}D = (V_{C2} + V_{C4} - V_{C1} - V_{C3} - V_{dc})(1-D) \tag{6}$$

$$V_{dc}D = (V_0 - V_{C1} - V_{C3} - V_{C5} - V_{dc})(1-D) \tag{7}$$

$$V_O = V_{C01} + V_{C02} = \frac{(1+N+T)V_{dc}}{1-D} \tag{18}$$

Rearranging equation (18), the overall voltage gain of the presented topology is obtained as

$$\text{Voltage Gain M} = \frac{V_O}{V_{dc}} = \frac{(1+N+T)}{1-D} \tag{19}$$

Considering a non-ideal CI with a coupling coefficient of k, the generalized expression for voltage gain is given by

$$M = \frac{V_O}{V_{dc}} = \frac{(1+N+kT)}{1-D} \tag{20}$$

4.2 Design of passive energy storage elements

The converter is expected to operate under continuous conduction mode (CCM) and the first stage is a conventional IBC stage. Therefore, the values of inductors and output capacitor is determined by considering the classical boost converter. Based on this, the design expressions for energy storage elements are given by

$$L_1 = L_{21} = \frac{V_{dc}D}{f_s \Delta I_L P} \tag{21}$$

$$C_{01} = C_{02} = \frac{I_O D}{\Delta V_C f_s} \tag{22}$$

where fs denotes switching frequency, ΔI_L is the inductor current ripple, P represents the number of interleaved phases and ΔV_C is the voltage ripple across the capacitor.

4.3 Voltage stress on switches

The voltage stress on the switch is the maximum voltage which the switch has to block during OFF state. Applying volt-second balance in loop formed by L1-S1-V_{dc} gives the switch voltage stress as

$$V_{S1} = V_{S2} = \frac{V_{dc}}{1-D} = \frac{V_{dc}}{6} = \frac{V_{dc}}{1+N} \tag{23}$$

Equations (19) and (23) evidently prove that though the output voltage is much higher than the input voltage, a switch with very low voltage rating can be used to obtain the required output voltage.

4.4 Voltage stress of diodes

By using equations (7), (15) and (16) and applying volt-second balance across inductors, the diode stresses are derived as

$$V_{D1} = V_{D2} = V_{D3} = V_{D4} = V_{D5} = \frac{2V_{dc}}{1-D} \quad (24)$$

$$V_{D6} = \frac{V_{dc}}{1-D} \quad (25)$$

Diodes D01 and D02 appear across the secondary winding of the CI stage. Hence, both these diodes have to block the voltage impressed across the secondary winding. Therefore, their voltage stress is given by

$$V_{D01} = V_{D02} = \frac{TV_{dc}}{1-D} \quad (26)$$

4.5 Resonant inductor and capacitor

ZVS turn ON of the switches S1 and S2 can be achieved due to resonance between the inductor (L_1, L_{21}) and the capacitors (C_{S1} and C_{S2}) added across the switches. For ease of design, L_1=L_{21}=L and C_{S1}=C_{S2}=C. Therefore, the resonant frequency is given by

$$f_{res} = \frac{1}{2\pi\sqrt{LC}} \quad (27)$$

The switching frequency f_s is chosen to be less than the resonant frequency f_{res} to enable ZVS turn ON of the switches.

5. Experimental Results

To demonstrate the practical feasibility of the presented converter, a prototype converter consisting of 1 CI and 5 DCM stages is built with the specifications provided in Table 1. The power rating was limited to 200W though in reality the CI based topology is capable of delivering much higher power. Photograph of the experimented prototype converter is shown in Fig.5. The experimental results were obtained using a Tektronix 4-channel isolated DSO (TPS2014B). Standard accessories such as high voltage probes and current probes were used at appropriate junctures to obtain the required voltage and current waveforms.

Table 1. Hardware prototype specifications

Parameter	**Symbol**	**Rating**
Input voltage	V_{in}	20V
Output voltage	V_o	360V
Output power	P_o	200W
Switching frequency	f_s	50kHz
Inductor	L1, L21	100μH
Turns ratio of CI	T	3
Number of DCM	N	5
Capacitors	$C_1 – C_5$	10μF/250V – Electrolytic
Output capacitor	C01, C02	47μF/500V – Electrolytic
Resonant capacitors	C_{S1}, C_{S2}	47nF/600V – Polystyrene
Switches	S1, S2	FDPF33N25T(250V/33A)
Diodes	D1 – D6	MUR1660 (600V/16A)
Diodes	D01, D02	1N5408

Fig. 6(a) shows the gate pulses applied to the switches S1 and S2 input voltage and the output voltage. For an input voltage of 20V, the desired voltage gain of 18 is obtained with a nominal duty ratio D=0.5 at a switching frequency of 50 kHz. This proves the validity of the converter design and synthesis. Fig. 6(b) shows the gate pulses, output voltage and current waveforms which demonstrate the power handling capability of the converter. Fig. 6(c) shows the voltage across the output capacitors C01, C02 and output voltage. The obtained voltage levels are in confirmation with the operating principle and design hypothesis. Fig. 7 shows the variation of inductor currents I_{L1} and I_{L21} with respect to the gate pulses V_{GS1} and V_{GS2} respectively. The magnitude of inductor currents are almost equal and 180 ° out of phase with respect each other. This phase shift results in cancellation of ripples at the input side, thus making the input current ripple free. Due to slight asymmetry and leakage inductance arising under practical conditions, the currents shared by the inductors is slightly non-uniform.

Fig. 8(a) shows the voltage stress across switches and the output voltage. The switch voltage stress is just a fraction of the output voltage. The voltage stress experienced by the diodes present in DCM stages is shown in Figs. 8(b) and 8(c). Fig. 8(d) shows the voltage stresses on the diodes present in CI stage. The complimentary behavior of the diodes D01 and D02 can be clearly verified. All the waveforms presented from Figs. 8(a) to 8(d) validate the proper operation of the DCM stages and the design methodology adopted. Since the voltage stress on the switches and diodes is only a fraction of the output voltage, devices with low voltage rating can be used to fabricate the converter. In addition, the voltage drops and thereby the power loss occurring across these elements can also be reduced.

The waveforms corresponding to efficiency computation when the converter operates under full load condition are shown in Fig. 9(a). The magnitudes of input and output parameters (voltage and current) are in accordance with the expected values. It is interesting to note that the input current is ripple free due to the interleaving technique.

Fig. 9(b) highlights the ZVS turn ON of the main switches S1 and S2. It is evident that voltages across the switches become zero when gate pulse is applied. In addition, only after the switch voltage has reached zero, currents through the respective switches begin to increase gradually. This is due to the addition of the soft-switching network comprising of capacitor and anti-body diode. The reverse current that flows through the anti-body diode for a short duration and clamps the switch voltage at zero, can also be observed. Due to reduced turn ON losses, higher efficiency compared to a hard switched counterpart is obtained as shown in Fig. 9(c). The converter operates at an efficiency of 95% while delivering 200W of power.

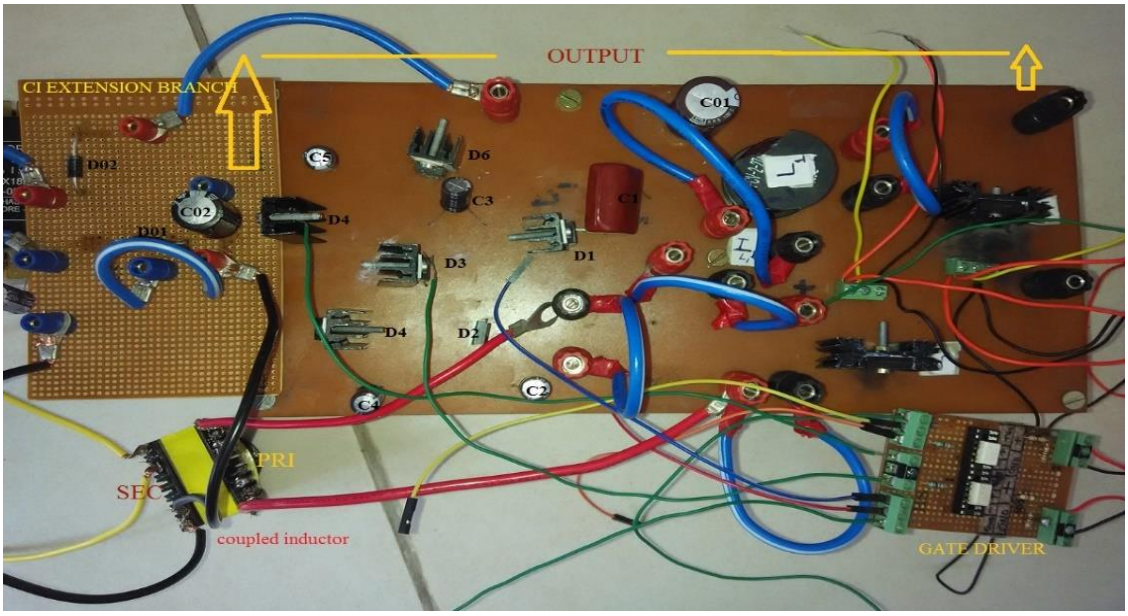

Fig.5. Hardware prototype of proposed converter with 5 DCM stages.

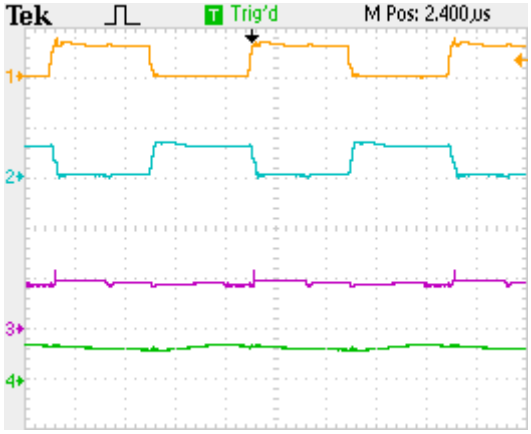

Fig.6. (a). Gate pulses, input and output voltage. Ch1: V_{GS1} (20V/div), Ch2: V_{GS2} (20V/div), Ch3: V_{dc} (20V/div), Ch4: V_o (500V/div), Time: 5µs/div.

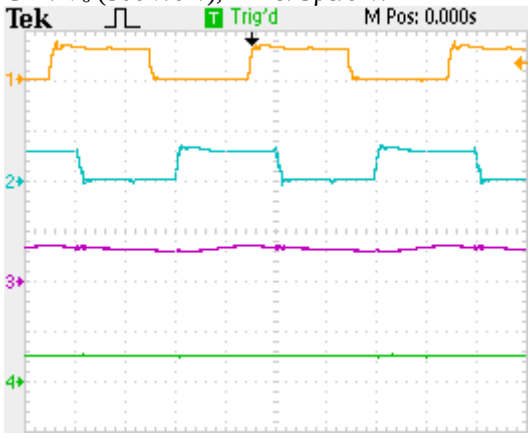

Fig. 6. (b) Gate pulses, output voltage and output current.

Ch1: V_{GS1} (20V/div), Ch2: V_{GS2} (20V/div), Ch3: V_o (500V/div), Ch4: I_o (1A/div), Time: 5µs/div.

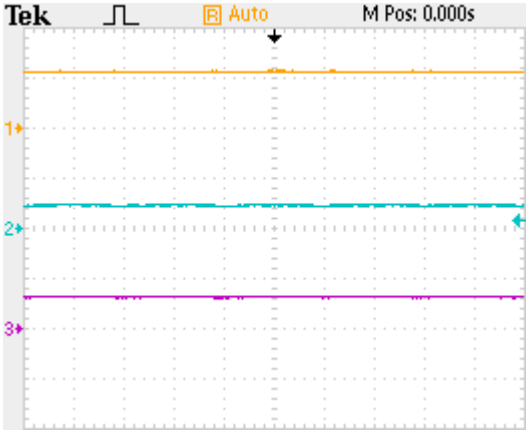

Fig.6 (c). Voltage across capacitors C01, C02 and output voltage V_o. Ch1: V_{C01} (200V/div), Ch2: V_{C02} (200V/div), Ch3: V_o (500V/div), Time: 5µs/div.

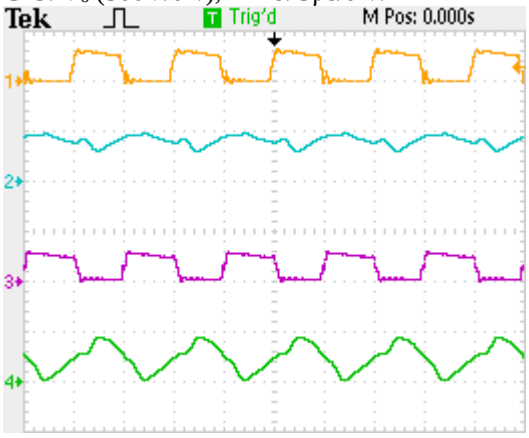

Fig.7. Gate pulses and inductor currents. Ch1: V_{GS1} (20V/div), Ch2: I_{L1} (5A/div), Ch3: V_{GS2} (20V/div), Ch4: I_{L21} (5A/div), Time: 10µs/div.

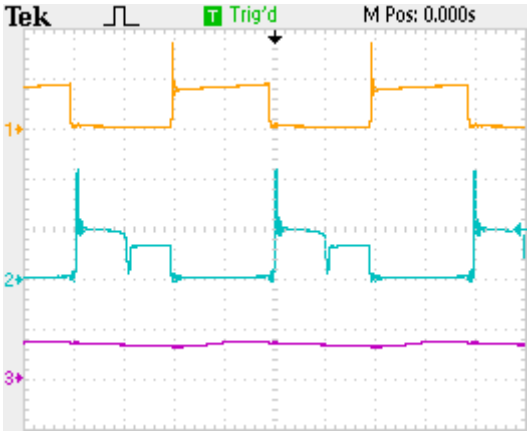

Fig. 8 (a). Voltage stress across switches and output voltage. Ch1: V_{DS1} (50V/div), Ch2: V_{DS2} (50V/div), Ch3: V_o (500V/div), Time: 5µs/div.

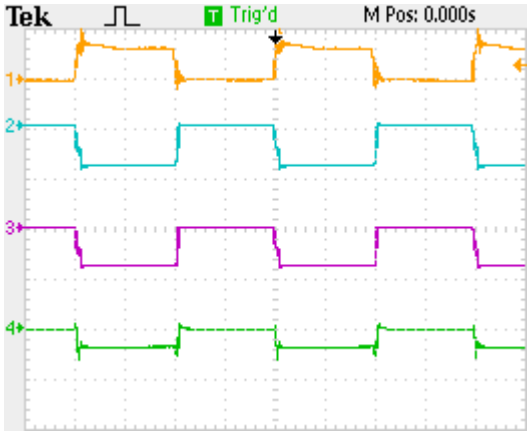

Fig. 8 (b). Gate pulse across S1 and voltage stress across diodes D2, D4 and D6. Ch1: V_{GS1} (20V/div), Ch2: V_{D2} (100V/div), V_{D4} (100V/div), V_{D6} (100V/div), Time: 5 µs/div.

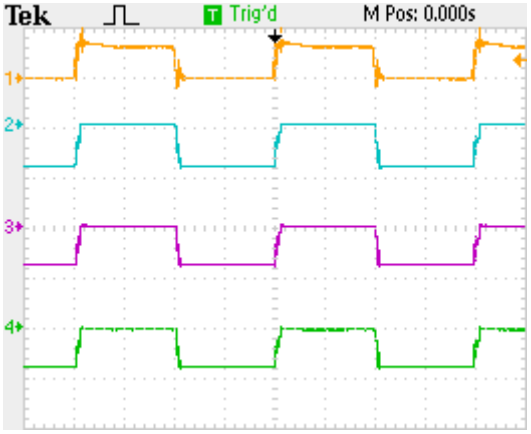

Fig. 8 (c). Gate pulse across S2 and voltage stress across diodes D1, D3 and D5. Ch1: V_{GS2} (20V/div), Ch2: V_{D1} (100V/div), V_{D3} (100V/div), V_{D5} (100V/div), Time: 5 µs/div.

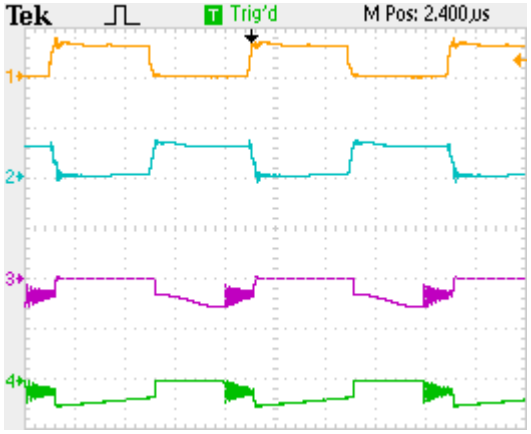

Fig. 8 (d). Gate pulse across S1, S2 and voltage stress across diodes D01 and D02. Ch1: V_{GS2} (20V/div), Ch2: V_{GS2} (20V/div), V_{D01} (200V/div), V_{D02} (200V/div), Time: 5 µs/div.

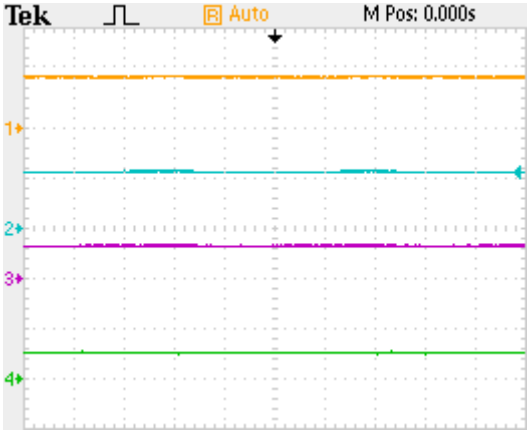

Fig. 9. (a) Input and output parameters. Ch1: V_{dc} (20V/div), Ch2: I_{in} (10A/div), Ch3: V_o (500V/div), Ch4: I_o (1A/div), Time: 5µs/div.

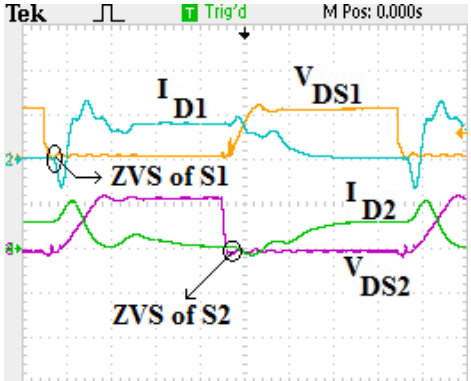

Fig.9 (b). ZVS switching of S1 and S2. Ch1 and Ch3: 50V/div, Ch2 and Ch4: 5A/div, T=2.5µs/div.

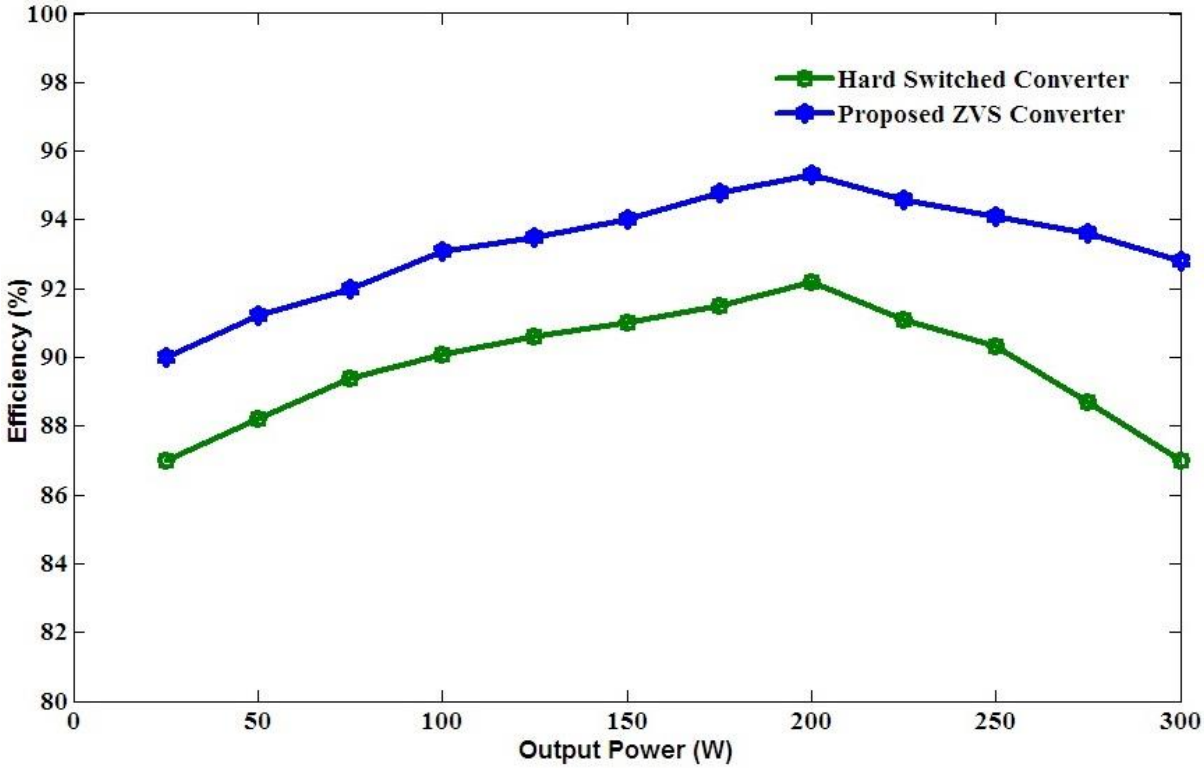

Fig.9 (c). Efficiency curve of the proposed converter

6. Conclusion

A CI based soft-switched interleaved high gain DC-DC converter which provides a high voltage conversion ratio has been developed, analysed, designed and practically demonstrated. By using 5 DCMs, 1 CI with a turns-ratio of 3 and operating the switches at 0.5 duty ratio, a voltage gain of 18 was obtained. Since DCMs were used as gain extension stages to enhance the overall voltage gain of the converter, both the switches and all the diodes experienced a very low voltage stress which was just a fraction of the output voltage. The operating efficiency of the converter was improved by employing ZVS technique. The converter operated at a full load efficiency of 95% while delivering 200W of power to the output. This topology is suitable for photovoltaic applications as the input current ripple is almost zero due to interleaving concept.

Acknowledgements

The authors wish to express their sincere thanks to all the faculty members, staff and student friends belonging to School of Electrical Engineering, VIT University, Chennai Campus for their help during the course of this work.

References

[1] Zahedi, "Solar photovoltaic (PV) energy: latest developments in the building integrated and hybrid PV systems", *Renewable Energy*, vol.31, pp. 711–718, 2006.

[2] R. J. Wai, W. H. Wang, and C. Y. Lin, "High-performance stand-alone photovoltaic generation system", *IEEE Trans. Ind. Electron.*, vol. 55, no. 1, pp. 240–250, Jan. 2008.

[3] C. Wang and M. H. Nehrir, "Power management of a standalone wind/photovoltaic/fuel cell energy system", *IEEE Trans. Energy Convers*., vol. 23, no. 3, pp. 957–967, Sep. 2008.

[4] Jansen Kai, W. Varvar, A. Groelinger, "The development of low cost amorphous silicon module technology for high-growth PV markets", *IEEE 33rd Photovoltaic Specialists Conf.*, 2008, pp. 1–5.

[5] R. J. Wai and W. H. Wang, "Grid-connected photovoltaic generation system", *IEEE Trans. Circuits Syst. I, Reg. Papers*, vol.55, no.3, pp.953–964, Apr. 2008.

[6] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC–DC converters", *IEEE Trans. Power* Lung-Sheng Yang, Tsorng-Juu Liang; and Jiann-Fuh Chen., "Transformerless DC–DC converters with high step-up voltage gain", *IEEE Transactions on Industrial Electronics*, vol.56, no.8, 3144-3152, 2009.*Electron.*, vol. 18, no. 1, pp. 65–73, Jan. 2003.

[7] Wuhua Li and Xiangning He., "Review of non-isolated high-step-up DC/DC converters in photovoltaic grid-connected applications", *IEEE Transactions on Industrial Electronics*, vol.58, no.4, 1239-1250, 2011.

[8] Taghvaee.M.H., Radzi. M.A.M., Moosavain.S.M., Hashim Hizam; and Hamiruce Marhaban.M., "A current and future study on non-isolated DC–DC converters for photovoltaic applications", *Renewable and Sustainable Energy Reviews*, vol.17, 216–227, 2013.

[9] Z. Qun and F. C. Lee, "High-efficiency, high step-up DC–DC converters", *IEEE Trans. Power Electron*., vol. 18, no. 1, pp. 65–73, Jan. 2003.

[10] D. A. Grant, Y. Darroman, and J. Suter, "Synthesis of tapped-inductor switched-mode converters", *IEEE Trans. Power Electron.*, vol. 22, no. 5, pp. 1964–1969, Sep. 2007.

[11] Lung-Sheng Yang, Tsorng-Juu Liang, Jiann-Fuh Chen, "Transformerless DC–DC converters with high step-up voltage gain", *IEEE Tran. Ind. Electron.*, vol. 56, no. 8, pp.314-3152, Aug. 2009.

[12] Y. Berkovich B. Axelrod, "Switched-coupled inductor cell for DC– DC converters with very large conversion ratio", *IET Power Electron*, vol. 4, no.3, pp. 309–315, 2011.

[13] Yun Zhang, Jian-Tao Sun, "Hybrid boost three-level DC–DC converter with high voltage gain for photovoltaic generation systems", *IEEE Trans., Power Electron.*, vol. 28, no. 8, pp.3659-3664, Aug. 2013.

[14] Wuhua Li, Weichen Li, Xin Xiang, Yihua Hu; and Xiangning He., "High step-up interleaved converter with built-in transformer voltage multiplier cells for sustainable energy applications", *IEEE Transactions on Power Electronics*, vol.29, no.6, 2829–2836, 2014.

[15] Ching-Tsai Pan, Chen-Feng Chuang, Chia-Chi Chu,, "A novel transformer-less adaptable voltage quadrupler DC converter with low switch voltage stress", *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp.4787-4796, Sep. 2014.

[16] Tohid Nouri, Seyed Hossein Hosseini, Ebrahim Babaei, Jaber Ebrahimi., "Interleaved high step-up DC-DC converter based on three-winding high-frequency coupled inductor and voltage multiplier cell", *IET Power Electronics*, vol.8, no.2, 175-189, 2015.

[17] Marcos Prudente, Luciano L. Pfitscher, Gustavo Emmendoerfer, Eduardo F. Romaneli, and Roger Gules, "Voltage multiplier cells applied to non-isolated DC-DC converters", *IEEE Trans. Power Electron.*, vol. 23, no. 2, 871-887, Mar. 2008.

[18] J.C. Rosas-Caro, J.M. Ramirez, A. Valderrabano, F.Z. Peng, "A DC–DC multilevel boost converter", *IET Power Electron.*, vol. 3, no.1, pp. 129–137, Nov. 2008.

[19] Ching-Tsai Pan, Chen-Feng Chuang, Chia-Chi Chu,, "A novel transformer-less adaptable voltage quadrupler dc converter with low switch voltage stress", *IEEE Trans. Power Electron.*, vol. 29, no. 9, pp.4787-4796, Sep. 2014.

[20] R. Girish Ganesan, M. Prabhakar, "Non-isolated high step-up interleaved boost converter", *Int. J. Power Electronics*, Vol. 6, No. 3, 2014.

[21] Luo-wei Zhou, Bin-xin Zhu, Quan-ming Luo, Si Chen, "Interleaved non-isolated high step-up DC/DC converter based on the diode–capacitor multiplier", *IET Power Electron.*, vol. 7, no.2, pp. 390–397, June. 2013.

[22] Li, W., He, X, "ZVT interleaved boost converters for high efficiency, high step-up DC–DC conversion", IET *Electrical Power Appl*., vol. 1, pp. 284–290, 2007.

[23] Y. Hsieh, T. Hsueh, and H. Yen, "An interleaved boost converter with zero-voltage transition", *IEEE Trans. Power Electron.*, vol. 24, no. 4, pp. 973–978, Apr. 2009.

[24] Hyun-Lark Do, "A Soft-Switching DC/DC converter with high voltage gain", *IEEE Trans. Power Electron*., vol. 25, no. 5, pp.1193-1200, May 2010.

[25] Ying-Chun Chuang, Yu-Lung Ke, Hung-Shiang Chuang; and Jung-Tai Chen., "A novel loaded-resonant converter for the application to DC-DC energy conversions", *IEEE Transactions on Industry Applications*, vol.48, no.2, 742–749, 2012.

[26] Hyun-Lark Do, "Improved ZVS DC-DC converter with a high voltage gain and a ripple-free input current", *IEEE Trans. Circuits ans Sys., I: Reg. Papers*, vol. 59, no. 4, pp.846-853, Apr. 2012.

[27] Sanghyuk, L., Pyosoo, K., Sewan, C, "High step-up soft-switched converters using voltage multiplier cells", *IEEE Trans. Power Electron.*, vol.28, no. 7, pp. 3379–3387, 2013.