Overcurrent Limitation for Digital Peak Current Mode DC-DC Converter

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Abstract-. The aim of this paper is to present an overcurrent limitation for the digital peak current mode dc-dc converter. The proposed method can detect the overcurrent in real time and it also maintains arbitrary current in the overcurrent limitation mode. It is expected to provide an effective function to protect the renewable energy system. The effectiveness of proposed method is confirmed from both simulated and experimental results.

Keywords dc-dc converter; overcurrent limitation; digital control; peak current mode.

1. Introduction

Digital control techniques have some advantages such as the flexibility of control and the cooperation of other systems. They are expected in the renewable energy system, for example, the photovoltaic solar system [1]-[4], wind power generation [5]-[7] and fuel cell/battery [8]. Since renewable energy sources influence dynamic characteristics of power converters, the peak current mode control is useful to obtain the high stability compared with the voltage mode control [9]-[11]. Therefore, it is widely used in various fields of renewable energy system. In the photovoltaic system, the peak current mode control has been used for the boost converter [12], [13], the buck converter [14], distributed flyback converters [15] and the SEPIC converter [16]. Also, the battery charger based on the peak current mode control has been reported in [17]. Along with the growing this research field, the protection techniques are also necessary for the reliable system. The overcurrent limitation for power converters is specifically important in order to protect from accidents [18]-[20].

The control of switching power converter is divided into the regulation mode and the overcurrent limitation mode. The regulation mode means that the output voltage is regulated to the desired value in the operation range. In the analog peak current mode control, the overcurrent limitation is easily realized by limiting the feedback value of output voltage connecting a zener diode only. The previous research [12]-[17] have used the analog peak current mode control.

On the other hand, it is difficult to implement the peak current mode control in the digital control. Since the digital control circuit has the delay time of A-D conversion and processing circuit, the peak current cannot be detected in real time like the analog control [21]. Although the predictive current mode control has been studied for digital control power converters [22]-[23], it has still the delay time for the prediction. Due to this, the digital peak current mode control does not seem a major control method. Furthermore, the overcurrent limitation method for the digital peak current mode control has not been reported yet. Thus, we have already reported a new peak current detector for the digital control dc-dc converter in the regulation mode [24], [25]. The peak current detector consists of an RC integrator and comparator. It can detect the peak current in real time. In this peak current mode control, the RC integration time represents the peak current because the start point of reactor current detection is close to the peak point. Therefore, the overcurrent limitation mode can be realized by using the RC integration time. Also, the load current is set to the arbitrary value in any load condition using the steady-state analysis.

This paper presents an overcurrent limitation method for the peak current mode dc-dc converter and its performance characteristics. It can achieve the superior overcurrent limitation performance using a simple additional circuit with the existing regulation mode. Once the overcurrent is sensed,

the overcurrent limitation mode calculates the digital control value from the steady-state analysis of peak current mode control for maintaining the limited current. Therefore, the proposed method can maintain arbitrary current by setting the limited current in the analysis formula. Moreover, it is obtained that the overshoot of reactor current is perfectly suppressed in the transient state. This paper is organized as follows. Section 2 describes the operation principle of the existing peak current mode control in the regulation mode. Also, the overcurrent detection and calculation parts are explained. In Section 3, the proposed overcurrent limitation characteristics are evaluated by simulated and experimental results in the steady-state and transient response. Finally, conclusions are described in Sec. 4.

2. Operation Principle

2.1. Summary of Existing Digital Peak Current Mode Control in Regulation Mode

In this study, the buck type dc-dc converter is used as the main circuit. Figures 1 and 2 show the circuit configuration and operation waveforms of the digital peak current mode dc-dc converter with the peak current detector [24]. E_i is the input voltage, e_o is the output voltage, i_L is the reactor current and I_o is the load current. In Fig. 1, the output voltage e_o is converted to the digital value $e_o[n]$ by the A-D converter. n denotes n-th switching period. $e_o[n]$ is used for the PID calculation for the output voltage regulation. The digital feedback value of output voltage N_{PID} is calculated as follows:

$$\begin{aligned} N_{PID}[n] = N_B &- K_P(e_o[n-1]-N_R) \\ &- K_I\sum(e_o[n-1]-N_R) \\ &- K_D(e_o[n-1]-e_o[n-2]) \end{aligned} \quad . \qquad (1)$$

where N_B is the reference bias value, N_R is the digital value of desired output voltage, K_P, K_I and K_D are the proportional, integral and derivative coefficients. N_B determines the operation bias point of dc-dc converter in the open loop.

$N_{PID}[n]$ is sent to the delay circuit of field-programmable gate array (FPGA). The delay circuit generates a signal S_D which determines the current sensing start time T_D based on $N_{PID}[n]$ as shown in Fig. 2. Equation 2 represents relationship between $N_{PID}[n]$ and T_D.

$$T_D = \frac{N_{PID}[n]}{N_{Ts}} T_s \qquad (2)$$

where T_s is the switching period and N_{Ts} is the digital value corresponding to T_s.

For the detection of i_L, the A-D converter is not necessary as shown in Fig. 1. Instead of the A-D converter, a simple detection circuit shown in Fig. 3 is used to detect the peak current. i_L is sensed by the sensing resistor R_S. The sensing voltage $e_S = R_S i_L$ is input to the peak current detector through the pre-amplifier. A_C is the gain of pre-amplifier.

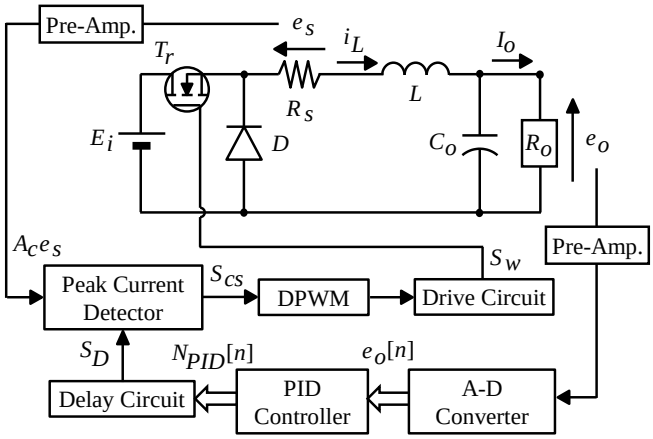


Fig. 1. Digital control dc-dc converter with proposed peak current mode control in regulation mode.

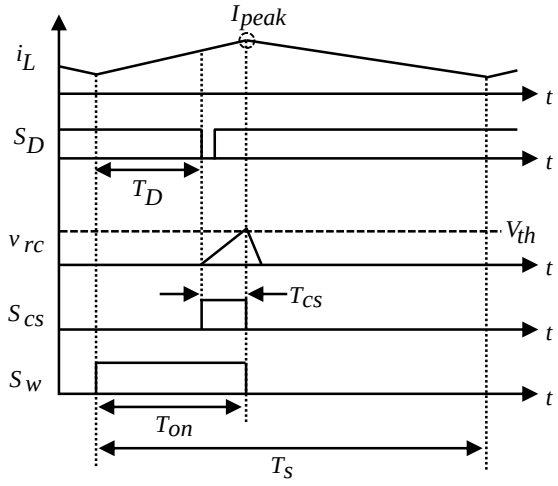


Fig. 2. Operation waveforms in regulation mode.

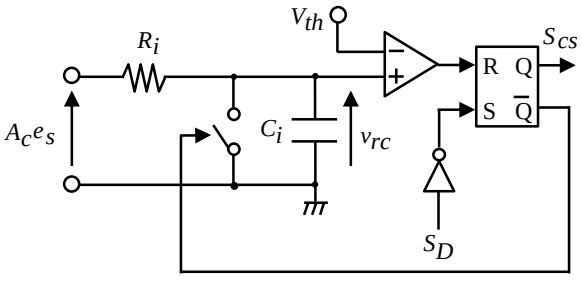


Fig. 3. Peak current detector.

$A_c e_S$ is input to the peak current detector which is composed of RC integrator and comparator as shown in Fig.

3. After S_D is turned off and the current sensing is started, v_{rc} is increased and S_{cs} is turned on. When v_{rc} reaches the threshold voltage V_{th}, S_{cs} is turned off. T_{cs} is the current sensing time in Fig. 2. In this moment, the peak current is detected. Equation (3) is obtained from Fig. 2 as follows:

$$\begin{aligned} v_{rc}(T_{on}) = V_{th} &= A_c R_S \frac{1}{T_{cs}} \int_0^{T_{cs}} i_L(t)dt \cdot \left\{1-\exp\left(\frac{T_{cs}}{\tau}\right)\right\} \\ &\approx A_c R_S \frac{1}{T_{cs}} \int_0^{T_{cs}} i_L(t)dt \cdot \left\{1-\left(1-\frac{T_{cs}}{\tau}\right)\right\} \\ &= A_c R_S \frac{1}{T_{cs}} \int_0^{T_{cs}} i_L(t)dt \cdot \frac{T_{cs}}{\tau} \end{aligned} \quad (3)$$

where $\tau = R_i C_i$ is the time constant in Fig. 3. When T_{cs} is much smaller than T_S, the following equation is obtained.

$$I_{peak} \approx \frac{1}{T_{cs}} \int_0^{T_{cs}} i_L(t)dt \quad (4)$$

Thus, I_{peak} is derived by substituting Eq. (3) into Eq. (4) as follows:

$$I_{peak} = \frac{\tau \cdot V_{th}}{A_c R_S T_{cs}}. \quad (5)$$

From this equation, the peak current detector can obtain the peak current value from T_{cs}.

2.2. Proposed Overcurrent Limitation Mode

Figure 4 shows the control circuit structure with the overcurrent limitation mode. The multiplexer (MUX), overcurrent detection part and N_{OC} calculation part are added to the regulation mode. As described in Sec. 2.1, the digital control value is only T_D in the proposed method. T_D is determined by N_{Drive}. T_D is calculated based on N_{PID} to keep the desired output voltage in the regulation mode even if the circuit state is the overload condition. In this case, I_O becomes more than the rated current. Therefore, a different calculation part, which is called N_{OC} calculation part, is necessary for the overcurrent limitation mode. The MUX is prepared to select $N_{PID}[n]$ or $N_{OC}[n]$. $N_{Drive}[n]$ is equal to $N_{PID}[n]$ in the regulation mode. When the overcurrent is detected, the smaller value of $N_{PID}[n]$ and $N_{OC}[n]$ is selected as $N_{Drive}[n]$. The overcurrent is detected by using T_{cs}. S_{OC} is the overcurrent detection signal. In the overcurrent limitation mode, the digital value N_{OC} calculates by using the steady-state analysis formula to keep the overcurrent limitation value I_{O_set}.

Figure 5 indicates the pattern diagram of overcurrent limitation characteristics of the proposed method in the steady-state. Table 1 shows definitions for key parameters in Fig. 5. R_1 is equal to $E_O{}^*/I_M$. The control mode is switched to the overcurrent limitation mode when R_O is smaller than R_1. I_O is limited to I_{O_set} and E_{O_OC} is changed by R_O in the overcurrent limitation mode. E_{O_OC} is calculated by I_{O_set} and R_O. The proposed overcurrent limitation method is realized by substituting E_{O_OC} into steady-state analysis formula. In the first step, the proposed method detects the overcurrent by using T_{cs}. In the second step, R_O is estimated and E_{O_OC} is calculated by I_{O_set} and the estimated load

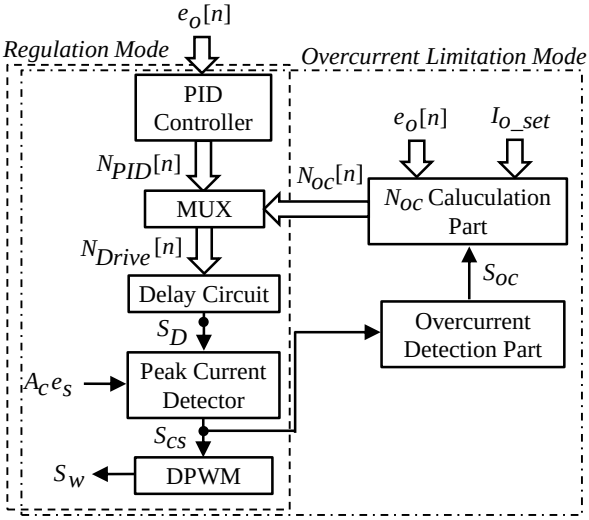


Fig. 4. Control circuit structure with the overcurrent limitation mode.

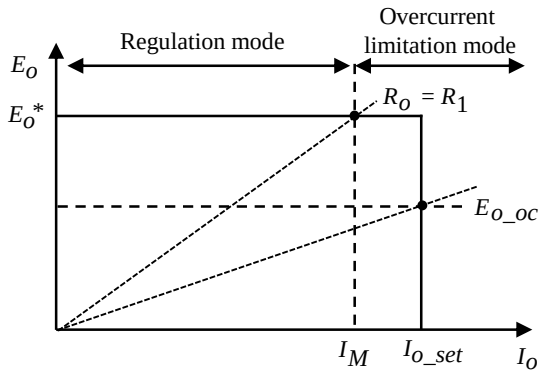


Fig. 5. Pattern diagram of overcurrent limitation characteristics of the proposed method.

Table 1. Key parameters in Fig. 5.

Desired output voltage in regulation mode	$E_O{}^*$
Overcurrent detection value	I_M
Limited current value	I_{O_set}
Output voltage when I_O is I_{O_set}	E_{O_OC}

value R_{o_est}. In the third step, T_D is calculated based on N_{oc} which is calculated by the steady-state analysis formula.

Figure 6 illustrates the overcurrent detection using T_{cs}. From Eq. (5), I_{peak} is obtained by T_{cs}. Thus, the proposed method sets T_{cs}* as the overcurrent detection value. S_{cs}* is a signal for the overcurrent detection. I_M is represented using

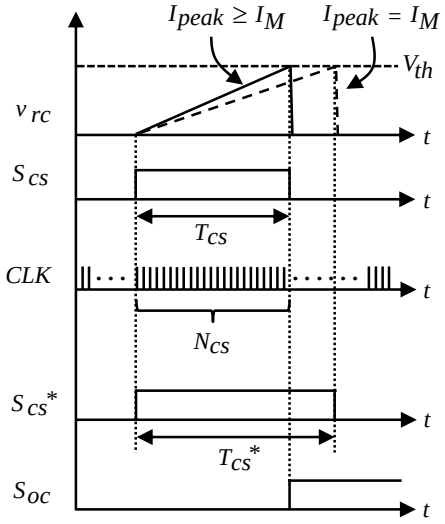


Fig. 6. Overcurrent detection using T_{cs}.

T_{cs}* as follows:

$$I_M = \frac{V_{th}}{A_C R_S T_{cs}^*}. \tag{6}$$

The FPGA calculates T_{cs} using the internal clock in every switching period. Equation (7) represents calculation for T_{cs}.

$$T_{cs} = N_{cs}[n] \cdot T_{clk} \tag{7}$$

where $N_{cs}[n]$ is the number of the internal clock cycle and T_{clk} is the clock period. When T_{cs} is smaller than T_{cs}*, the overcurrent detection signal S_{oc} is turned on and the operation mode is shifted to the overcurrent limitation mode.

Once the overcurrent is detected, the MUX selects the smaller value of $N_{PID}[n]$ and $N_{oc}[n]$ as $N_{Drive}[n]$ in order to change the operation mode smoothly. When $N_{oc}[n]$ is smaller than $N_{PID}[n]$, T_D is obtained as follows:

$$T_D = \frac{N_{Drive}[n]}{N_{Ts}} T_s = \frac{N_{oc}[n]}{N_{Ts}} T_s. \tag{8}$$

$N_{oc}[n]$ is calculated based on the steady-state analysis of proposed peak current mode control as following. From Fig. 2, T_D is given as

$$T_D = T_{on} - T_{cs}. \tag{9}$$

In the buck type dc-dc converter, T_{on} is solved as following:

$$T_{on} = \frac{E_o + (r + R_S) I_o}{E_i} T_s. \tag{10}$$

where r is the internal loss of dc-dc converter without R_S.

T_D is obtained by substituting Eqs. (5) and (10) into Eq. (9).

$$T_D = \frac{E_o + (r + R_S) I_o}{E_i} T_s - \frac{\tau \cdot V_{th}}{A_C R_S I_{peak}}. \tag{11}$$

Here, following equations are obtained in the steady-state of buck type dc-dc converter.

$$I_o = \frac{E_i - E_o}{2L} T_{on} + I_v \tag{12}$$

$$I_v = I_{peak} - \frac{E_i - E_o}{L} T_{on} \tag{13}$$

where I_v is the value of valley inductor current. From Eqs. (12) and (13), I_{peak} is obtained as following:

$$I_{peak} = I_o + \frac{E_i - E_o}{2L} T_{on}. \tag{14}$$

T_D is represented by substituting Eq. (14) into Eq. (11).

$$T_D = \frac{E_o + (r + R_S) I_o}{E_i} T_s - \frac{\tau \cdot V_{th}}{A_C R_S} \cdot \frac{1}{I_o + \frac{E_i - E_o}{2L} \cdot \frac{E_o + (r + R_S) I_o}{E_i} T_s}. \tag{15}$$

By using E_{o_oc} and I_{o_set} for the overcurrent limitation mode, Eq. (15) is rewritten as

$$T_D = \frac{E_{o\_oc} + (r + R_S) I_{o\_set}}{E_i} T_s - \frac{\tau \cdot V_{th}}{A_C R_S} \cdot \frac{1}{I_{o\_set} + \frac{E_i - E_{o\_oc}}{2L} \cdot \frac{E_{o\_oc} + (r + R_S) I_{o\_set}}{E_i} T_s}. \tag{16}$$

From Eq (16), T_D is obtained by determining E_{o_oc} and I_{o_set} in the overcurrent limitation mode because other values are constant.

N_{oc} is calculated from (8) and (16) as following:

$$N_{oc}[n] = \frac{E_{o\_oc} + (r + R_S) I_{o\_set}}{E_i} N_{Ts} - \frac{\tau \cdot V_{th}}{A_C R_S T_s} \cdot \frac{N_{Ts}}{I_{o\_set} + \frac{E_i - E_{o\_oc}}{2L} \cdot \frac{E_{o\_oc} + (r + R_S) I_{o\_set}}{E_i} T_s}.$$

(17)

The unknown variable is only E_{O_oc} in Eq. (17). E_{O_oc} is calculated by I_{O_set} and R_O. Although R_O is obtained by E_O and I_O in the steady-state, the proposed method uses I_{peak} instead of I_O because I_O is not detected. The estimated load value R_{O_est} is given by

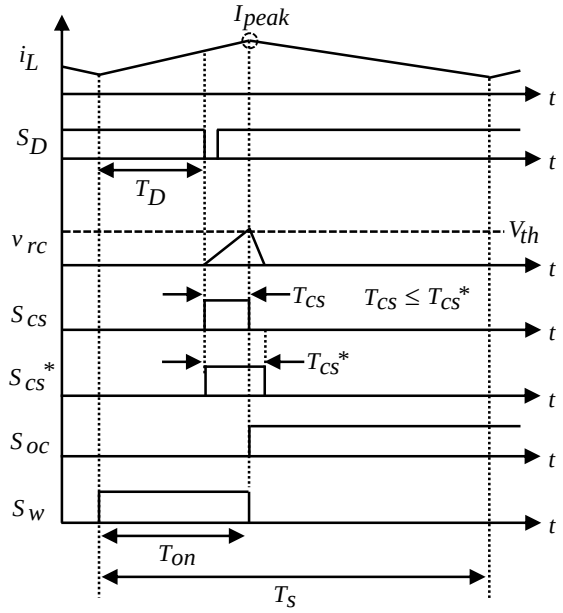


Fig. 7. Operation waveforms in overcurrent limitation mode.

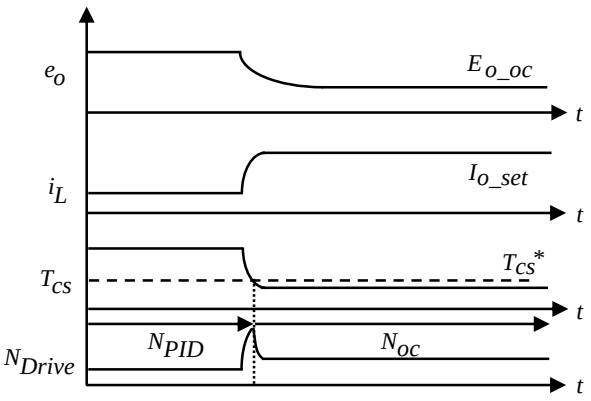


Fig. 8. Overcurrent limitation mode in transient state.

$$R_{O\_est} = \frac{E_O}{I_{peak}} = \frac{e_O[n]}{G_V \cdot I_{peak}} . \quad (18)$$

where G_V is the conversion gain from the analog value of output voltage to the digital one. G_V includes the gain of the pre-amplifier and the A-D converter. E_{O_oc} is derived as

$$E_{O\_oc} = R_{O\_est} \cdot I_{O\_set} . \quad (19)$$

By substituting Eq. (19) into (17), N_{oc} is calculated to maintain the load current as I_{O_set} in the overcurrent regulation mode.

Figure 7 shows operation waveforms in the overcurrent limitation mode. As mentioned above, the proposed overcurrent limitation method sets T_{cs}*. T_{cs} is compared with T_{cs}* by using S_{cs} and S_{cs}*. T_{cs} is larger than T_{cs}* in the regulation mode. T_{cs} becomes small with increasing i_L. When T_{cs} reaches T_{cs}*, S_{oc} is turned on in order to switch the control mode from the regulation mode to the overcurrent limitation mode.

Figure 8 shows operation waveforms of the overcurrent limitation mode in the transient state. T_{cs} is decreased with increasing i_L. the overcurrent detection is performed by T_{cs}. After the overcurrent detection, N_{oc} is selected as N_{Drive} to maintain I_{o_set}.

3. Overcurrent Limitation Characteristics

Table 2 shows circuit parameters for the main and control circuits. The digital control circuit is implemented by a Xilinx Vertex-5 FPGA. The A-D converter for e_o is 14bits. K_P, K_I and K_D are determined from the regulation characteristics and the load step change from 0.5A to 1A in the regulation mode. As long as E_o can be kept to E_o* in the steady-state of regulation mode, these coefficients do not have an influence on proposed overcurrent limitation characteristics. The circuit simulator is PSIM. Since the duty ratio is always controlled to be less than 0.5 in this study, the slope compensation is not performed.

Table 3 shows simulated results of R_{O_est} in the steady-state when I_{O_set} is 1.2A and 1.4A. The error rate between R_O and R_{O_est} is less than 8%. Thus, the proposed method can estimate the load value from Eq. (18).

Figure 9 illustrates the overcurrent limitation characteristics of simulated results when I_{O_set} is 1.2A and 1.4A. The operation range of I_O is from 0.2A to 1A in the regulation mode because the current mode control is generally switched to the voltage mode control in the light load condition. Good regulation characteristics are ensured

Table 2. Circuit parameters for main and control circuits.

Parameter	Value	Parameter	Value
E_i	15 V	K_P	5
E_o*	5 V	K_I	0.06
L	175 μH	K_D	1
C_o	285 μH	T_{clk}	10 ns
R_S	0.05 Ω	A_c	128
r	0.2 Ω	τ	2.75 μs

T_s	10 μs	V_{th}	0.8 V
G_v	500	I_M	1 A
N_{Ts}	10000	T_{cs}*	330 ns
N_B	2950	I_{o_set}	1.2A or 1.4A
N_R	2500		

Table 3. Simulated results of R_{o_est} in steady-state.

R_o	R_{o_est}	
	I_{o_set} = 1.2 A	I_{o_set} = 1.4 A
3 Ω	3.12 Ω	3.11 Ω
2 Ω	2.12 Ω	2.09 Ω
1 Ω	1.08 Ω	1.07 Ω

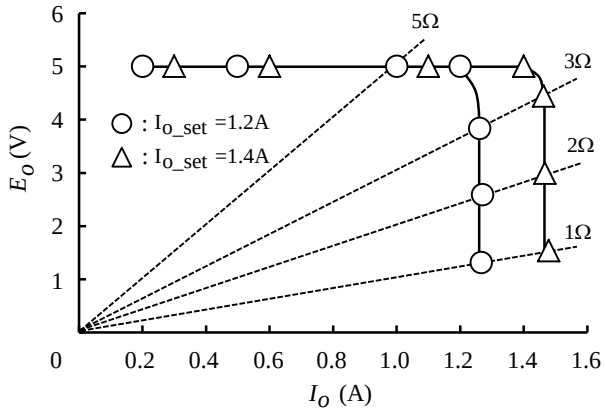


Fig. 9. Overcurrent limitation characteristics when I_{o_set} is 1.2A and 1.4A.

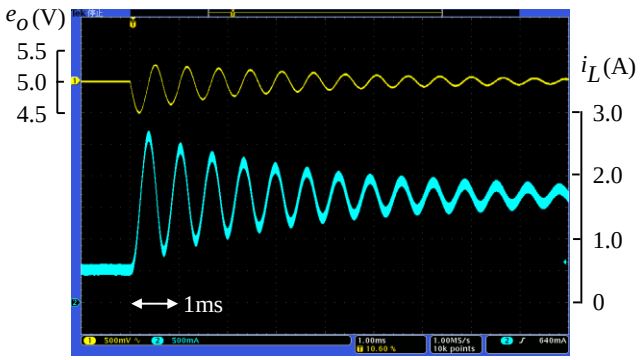
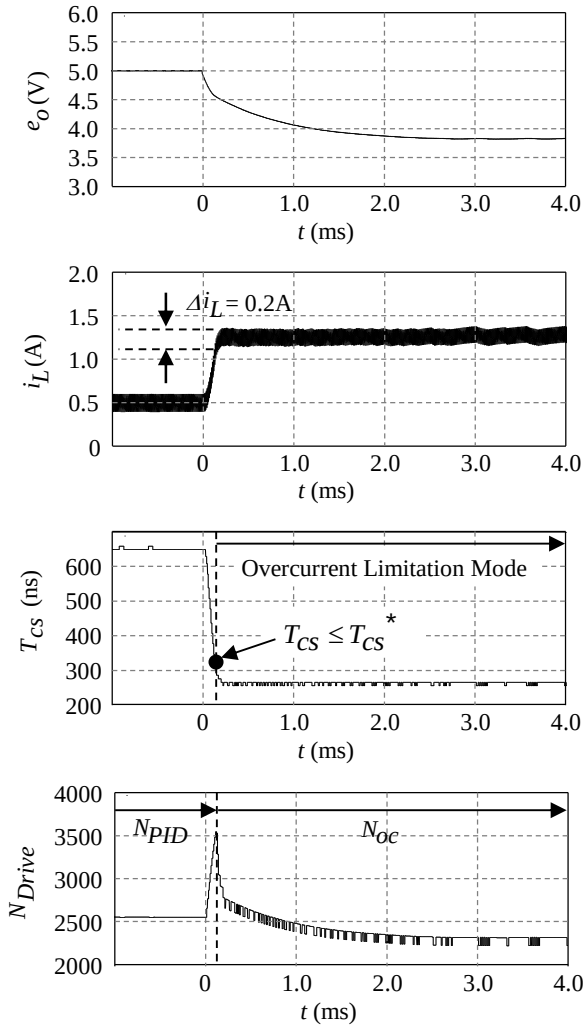


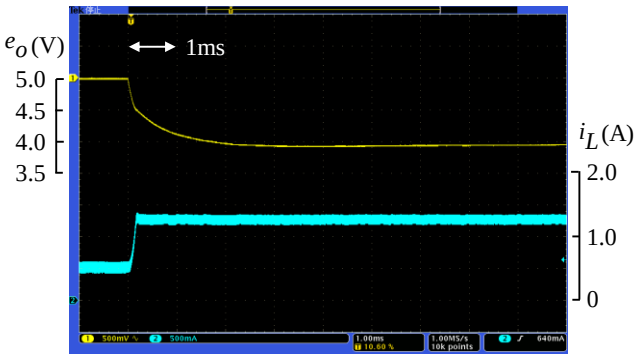
Fig. 10. Transient response without the overcurrent limitation when the load step change is from 10Ω to 3Ω.

in the regulation mode. When R_o is set to 3, 2 and 1Ω, I_o is maintained I_{o_set} by the proposed method. The error rate between I_o and I_{o_set} is less than 6% in the overcurrent limitation mode. It is verified that the proposed overcurrent limitation mode can keep arbitrary current by changing I_{o_set}.

Figure 10 shows the experimental result of transient response without the overcurrent limitation when the load step change is from 10Ω to 3Ω. e_o is converged to E_o* in the



(a) Simulated result.

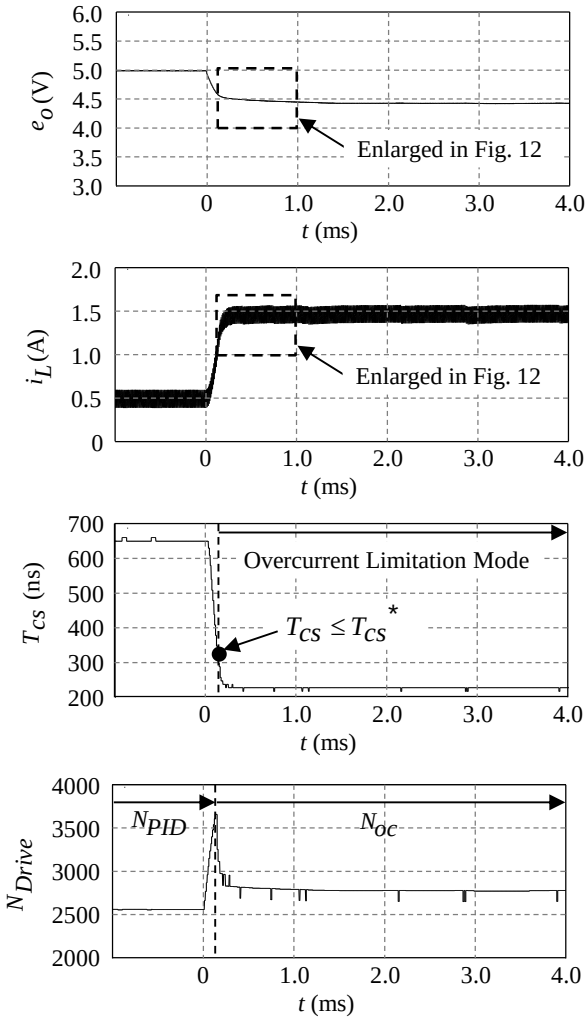


(b) Experimental results.

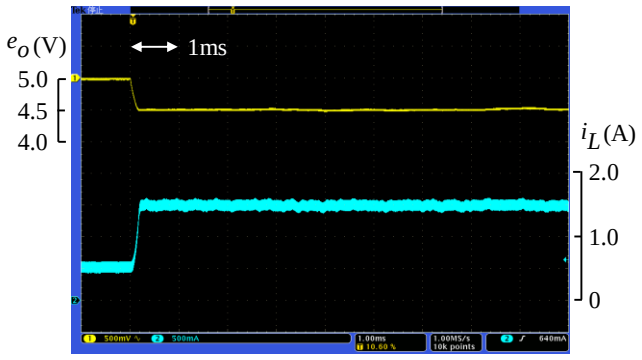
Fig. 11. Transient response with the overcurrent limitation when I_{o_set} is 1.2A.

regulation mode even if R_o is small value. Since E_o* is 5V and R_o is 3Ω, I_o becomes 1.67A in the steady-state. Moreover, the large overshoot of i_L is occurred and it is 2.7A.

Figure 11 shows the transient response with the proposed overcurrent limitation when I_{o_set} is 1.2A. The load step change is from 10Ω to 3Ω. The simulated and experimental results are well matched. Before the load step change, the control mode is the regulation mode and N_{Drive} is equal to N_{PID}. N_{Drive} is 2687 in this case, that is, T_D is 2.687μs from Eq. (2) and Table 2. Since i_L is increased and e_o is decreased after the load step change, T_{cs} is decreased and N_{Drive} (=N_{PID}) is increased, respectively. The control mode



(a) Simulated result.



(b) Experimental results.

Fig. 12. Transient response with the overcurrent limitation when I_{o_set} is 1.4A.

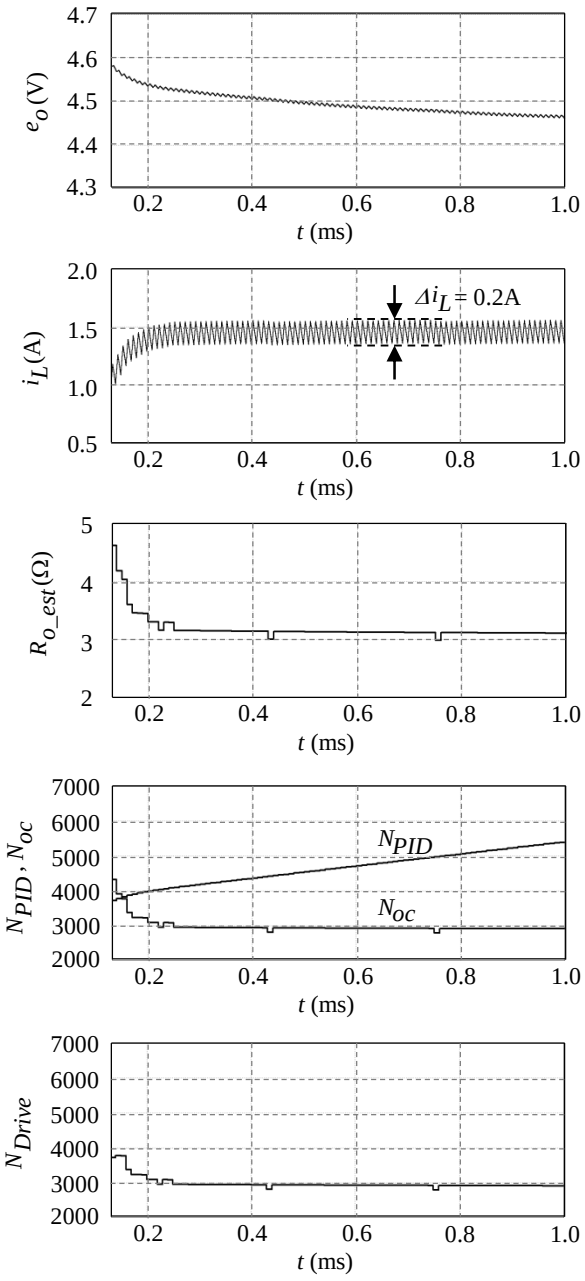


Fig. 13. Enlarged waveforms of transient response with the overcurrent limitation when I_{o_set} is 1.4A.

is changed from the regulation mode to the overcurrent limitation one when T_{CS} is less than T_{CS}*. In the overcurrent mode, N_{Drive} is equal to N_{OC}. Therefore, the overcurrent is not occurred because I_O becomes the constant to I_{O_set}. It is confirmed that the proposed method keep the limited current. Furthermore, the overshoot of i_L is not occurred compared with Fig. 10.

Figure 12 shows the transient response with the proposed overcurrent limitation when I_{O_set} is changed to 1.4A. The load step change is the same with Figs. 10 and 11. As well as Fig. 11, i_L is smoothly converged to I_{O_set} without the overshoot.

Figure 13 is enlarged views of Fig. 12 from the beginning of the overcurrent limitation mode, and it also shows R_{O_est}, N_{PID} and N_{OC} in the simulated result. Since e_O is decreased in the overcurrent limitation mode, N_{PID} is increased. N_{OC} is chosen to N_{Drive} when N_{OC} is becomes smaller than N_{PID}. R_{O_est} is calculated by using $e_O[n]$ and I_{peak} in every switching cycle. R_{O_est} shows the larger value than 4.5Ω at the beginning of the overcurrent limitation mode. When e_O decreases and i_L decreases in the transient state, R_{O_est} becomes close to 3 Ω. The overcurrent limitation mode calculates N_{OC} which can maintain I_{O_set} by using the value of R_{O_est} updated in every switching period. Furthermore, the reactor current ripple Δi_L is 0.2A as shown in Fig. 13. Thus, the difference of I_{peak} and I_O is 0.1A. Since Δi_L is very small and I_{peak} is close to I_O, the switching stress is very few.

As a result, the overcurrent limitation method can be implemented for the digital peak current mode dc-dc converter. It is revealed that the proposed method has superior overcurrent limitation characteristics.

4. Conclusion

The overcurrent limitation for the digital peak current mode dc-dc converter is presented in this paper. The proposed overcurrent limitation can be easily realized by using the existing function and the simple additional circuit. The overcurrent is quickly detected by using the integration time of peak current detector. The proposed method can maintain arbitrary current in the overcurrent limitation mode. Moreover, the overshoot of reactor current is not occurred in the transient response. In the renewable energy system, digital control dc-dc converter will be increased for the cooperation with other systems. Therefore, the proposed overcurrent limitation method is expected to provide an effective function to protect such system. The effectiveness of the proposed method is revealed by simulated and experimental results.

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