Passive Islanding Detection Method based on Resultant Sequence Impedance Component and Load Shedding in Islanded Area

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Abstract- The active island detection method aims to reduce the blind area of passive island detection methods, thereby affecting power quality. The concept of integrated sequential impedance is offered as a new approach to island detection. This method replaces the conventional impedance approach's abrupt variable with the integrated impedance sequence component of the Inverter side union point. Islanding is detected when the value exceeds the threshold range by monitoring the PCC for a shift in the integrated impedance sequence component. The authors recommend implementing a priority-based load shedding strategy to address the power mismatch in the identified islands. To prevent accidental tripping, it offers superior stability in a variety of non-islanding scenarios. Other benefits of the proposed approach include its low cost and ease of implementation, independence from the number and type of DG connected to the utility grid, and the absence of any negative effects on output power quality. The efficacy of the proposed method has been confirmed through studies conducted in various real-world settings. Compared to other methods reported in the literature, the obtained detection times show that the proposed method is superior.

Keywords. Islanding detection; Distributed generation; Sequence components; Non detection zone; Load shedding

Nomenclature

PCC	Point of common coupling	IDW	Islanding detection waveform
NIS	Non islanding	LS	Load Shedding
DG	Distributed generation	Q.F	Quality factor
NDZ	Non detection zone	RPV	Reactive power variation
SMS	Slip mode frequency shift	LLL	Three phase fault
ROCOF	Rate of change of frequency	LL	Line to line fault
AIP	Active islanding protection	LG	Line to ground fault
AI	Artificial intelligence	PC	Power control
SP	Signal processing	T	Transformation matrix
PV	Photovoltaic	a	Phase rotation operator
RSIC	Resultant equence impedance component	V_{abc}	Three phase supply voltage

V_{abc}^{1}	Positive sequence components
V_{abc}^{2}	Negative sequence components
V_{abc}^{0}	Zero sequence components
$Z_2 = \frac{V_a^2}{I_a^2}$	Negative sequence impedance
$Z_1 = \frac{V_a^1}{I_a^1}$	Positive sequence impedance
Z_{norm}	Sum of positive and negative sequence impedances
Z_{inst}	Instantanious impedance of positive and negative sequence components
PC	Priority coefficient on specified bus
k	Is the bus number
$f_{k,t}$	Frequency at k^{th} bus
$f_{\text{int},0}$	Initial frequency after islanding
$v_{k,t}$	Voltage when load shedding started
$v_{\text{int},0}$	Initial voltage in islanded area

1. Introduction

Experts in the power industry are very interested in DG of alternative energy as a possible solution to environmental challenges. Integrating DG networks also presents numerous security and protection issues. When DGs keep running despite the lack of access to the power grid, this perpetuates a problem known as islanding. If the DGs can't maintain voltage and frequency on their own, it could cause several problems for the system, including a decline in stability and power quality. Due to the unfavorable effects of widespread islanding caused by DG penetration. When a DG is cut off from the grid but its loads are still plugged in, the result is an island [1]. This occurred when this section of the grid was accidentally cut off from the rest of the system. Because of the risks to maintenance workers, inadvertent islanding occurrences should be avoided in power systems. Experts have warned that this phenomenon poses a significant threat to the safety of the users, grid, and island's inverters. The idea of islands has developed in recent decades. Short islanding (lasting less than one second) and unintended islanding (lasting more than one second) were identified. To protect users and infrastructure, early islanding situation detection is crucial [2-3]. There are three main types of islanding detection methods: passive methods, active methods, and communication-based methods [4]. Power line connection, supervisory control, and data collecting are only a few examples of remote technologies that rely on two-way communication between utilities and DGs. These systems require a dependable communication link but are costly to build because they lack an NDZ [5-6]. Islanding detection approaches don't function because of loading conditions like NDZs [7]. Because of this, NDZs are unable to forestall the phenomenon of islanding. One's attitude towards local methods can be aggressive or passive. Measurement of DG properties at the regional level and comparison to reference values is the backbone of passive methods. Over/under frequency/voltage protection, phase jump detection, and voltage harmonic monitoring are all examples of popular passive approaches [8-9]. The NDZ for these tactics is quite big. Active strategies to deal with the NDZ problem are gaining in favors. Islanding is identified when the grid becomes unstable due to the introduction of disturbances into the system's operational control. Active approaches benefit irreversibly from a smaller NDZ and a shorter time to detection. Active methods include voltage shift, negative sequence current injection, SMS, Sandia frequency [10-11].

While the NDZ for active approaches is small, there is a significant risk of erroneous detection when several DGs are present since the injection parameter will overlap with events that are not islanding. Although the NDZ is small, the problem arises due to the injection parameter's overlap with occurrences that do not include an island. Compared to passive methods, the NDZ is often smaller in active AIP methods, which are based on intentionally injecting perturbations to cause voltage magnitude or frequency to drift outside of the established thresholds. Because active approaches rely on purposefully introducing the disturbances, this is the case [12-13]. However, this enhanced islanding detection performance comes at the expense of the power quality provided by active approaches. The NDZ issue does not impact communication-based methods, although they tend to be expensive. Detection techniques have advanced by combining active and passive procedures or their variations. These strategies combine elements of other approaches. Among these methods are the Improved Active frequency drift anti islanding detection method [14], and the Hybrid islanding detection method for inverter-based DGs using reactive power injection and ROCOF [15], to name a few. In contrast to many other active AIP schemes, current distortion is not an issue with RPV-based AIP techniques. In addition to being more cost-effective, manipulating the DG unit's reactive power output rather than its active power is an option worth considering [16]. The frequency variation over time is one of the criteria used to identify islanding. Many of the active methods' threshold settings and major coefficients are difficult to calculate or select [17-18]. Certain methods can negatively affect power quality, such as injecting current, active power, or reactive power [19]. Modern techniques employ a feedback loop to increase the stability of the detecting process. When the frequency is being monitored, detection times increase [20] and decrease [21]. Ten electrical cycles are sometimes required for islanding detection [22].

The most up-to-date passive method utilizes the ripple spectrum content of the voltage at the PCC to detect islanding in less than 300 ms (18 electrical cycles) [23]. It is highly reliable, can detect islanding even when there is no variation in power, and is simple to set up, among many other advantages over passive and active systems. Ripple content is strongly dependent on the operating frequency of the inverter (DC-DC converter), hence the method is not broadly applicable irrespective of the size and specifications of the DG system. Adding a high-powered inverter to the grid may increase the ripple in the instantaneous output voltage as measured by the PCC, which in turn could lead to late detections. Therefore, avoiding calculations with a large period window can help shorten the time required for detection.

Impedance measuring techniques have been used to identify islanding in a number of patents and published methodologies. "Signal Injection "and "Variations in the Voltage and Frequency" [24] are three examples of these approaches. In [24], injecting a single non-harmonic frequency into a circuit was a reliable way to evaluate impedance. The non-harmonic frequency injection method has shown to be effective; however, this approach has a number of drawbacks, including complicated integration, high injection power requirements, disruptive injections, and expensive interface with the power network. This research likewise employs an approach based on impedance measurements, but instead of testing at other frequencies, we do it at the fundamental frequency by taking advantage of unbalanced conditions already existing in the power network or by injecting small unbalanced signals.

Both islanding detection and impedance measurement have previously made use of similar strategies based on the use of unbalanced situations. Authors in [25-26] described injecting and measuring negative sequence current for islanding detection in simulation using a controlled voltage source inverter. Rapid islanding detection in under 60 ms (3.5 cycles) was made possible by injecting a negative-sequence current of 2% to 3%. The stability of an onboard impedance network can also be monitored using an unbalanced source [27-29]. In summary, various passive islanding detection techniques are not well-suited to handle cases where the power output from DGs and the power input from loads are identical. Non-islanding scenarios, such as switching loads or a short circuit, can also cause most algorithms to fail. There have been both passive and active approaches to this problem, however the active approaches risk damaging the power quality of the system by adding noise where it isn't needed [30-31]. Hybrid systems give more reliable and efficient performance than active and passive approaches, but at the cost of a longer detection time and a more substantial calculation burden. Combining SP and AI-based methods with passive-based methods can improve accuracy [32-33]. However, retraining AI-based approaches is a major drawback of these systems, and SP-based techniques may not be able to reduce the NDZ.

In this research, we propose a new approach to detecting islanding by utilizing the impedance sequence. The symmetric component approach requires monitoring voltage and current fluctuations at the common connection point in order to segment the three-phase current voltage into sequence components. The islanding can be determined by comparing the nominal impedance sequence components before and after the islanding manifestation. The impedance sequence component is the ratio of the voltage sequence component to the current sequence component during a disturbance. Unlike some other methods, this one does not introduce harmonics that degrade power quality or disrupt the interaction between inverters. The method can detect isolated islands just two cycles after they have developed, and it has a higher detection efficiency overall. It is obvious that the voltage and current will fluctuate until the isolated island state runs steadily, at which point they will be decomposed using the symmetric component approach, since the PCC voltage and current cannot change when an isolated island originates. The following is the structure of this article: Section 2 covers the IEEE -13 bus test system and the proposed algorithm for the suggested technique. Section 3 explored the outcomes and implications of the proposed method. Finally, Section 4 concludes.

2. Test System and Proposed Method

2.1 Architecture and Control Scheme

The IEEE Power Engineering Society developed the 13-node distribution test feeder to standardise the testing of distribution networks. The distribution feeder runs at a frequency of 60 hertz and a voltage of 4.16 kV. The test feeder in a distribution system simulates elements including transmission lines, underground cables, spot loads, distributed loads, capacitors, transformers, and regulators. The modified IEEE 13-node distribution test feeder is illustrated in Figure.1 and explained in more detail in the aforementioned publication [24]. In the upgraded test system, distributed generators (DGs) like wind and solar PV power plants are connected to the grid via nodes 646, 611, and B675.

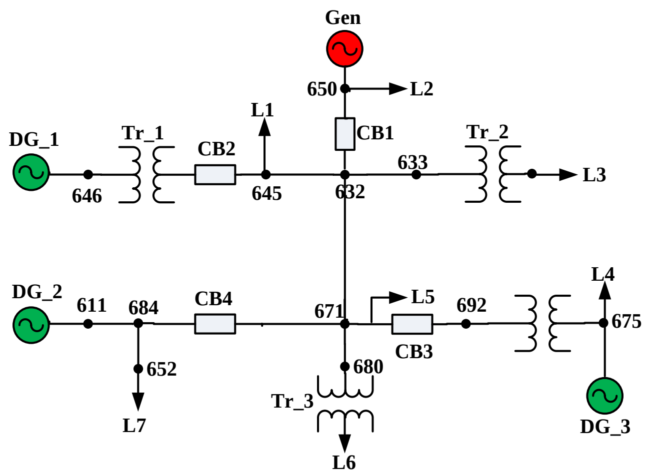


Fig. 1. System under consideration for proposed islanding detection technique.

2.2 The Proposed Islanding Detection Technique

The proposed islanding detection method in time series components and RSIC are described as follows

2.2.1 Symmetrical Components in Time Domain:

The concept of symmetric components was first introduced by in [25] to study unbalanced ploy-phase networks. An unbalanced three-phase system's steady-state phases (V_{abc}) are broken down into a positive (V_{abc}^1), negative (V_{abc}^2) and zero sequence (V_{abc}^0) collection using this method, as shown in Eq. (1)

$$V_{abc} = V_{abc}^1 + V_{abc}^2 + V_{abc}^0 \tag{1}$$

As a result, given a standard three-phase voltage matrix, V_{abc}, is shown in equation (2), we can derive the phase "*a*" symmetric components via the equation $T_S = TV_{abc}$. Where $V_S = [V_a^1, V_a^2, V_a^0]^T$ and *T* is the transformation matrix [32].

$$\begin{bmatrix} V_a^1 \angle \theta_a^1 \\ V_a^2 \angle \theta_a^2 \\ V_a^0 \angle \theta_a^0 \end{bmatrix} = \frac{1}{3} \begin{bmatrix} 1 & a & a^2 \\ 1 & a^2 & a \\ 1 & 1 & 1 \end{bmatrix} \begin{bmatrix} V_a \angle \theta_a \\ V_b \angle \theta_b \\ V_c \angle \theta_c \end{bmatrix} \tag{2}$$

Where $a = e^{j120^0}$

Phase's *b* and *c* have the following sequence components are shown in equation (3)-(5)

$$V_b^1 = a^2 V_a^1; \qquad V_c^1 = a^2 V_a^1 \tag{3}$$

$$V_b^2 = a^2 V_a^2; \qquad V_c^2 = a^2 V_a^2 \tag{4}$$

$$V_a^0 = V_b^0 = V_c^0 \tag{5}$$

2.2.2 Resultant Sequence Impedance Component (RSIC)

One difficulty with impedance-based islanding detection is determining the equivalent impedance at the common point. The inverter causes a change in the system's characteristic current, and the non-characteristic harmonic voltage is then measured to establish the system's impedance to these harmonics. The conventional approach has two major flaws: (1) it compromises power quality under normal conditions of use by injecting harmonic current into the system. (2) Parallel operation of the multi-inverter results in mutual influence from the harmonics injected by each inverter. These could lead to more mistakes or blind spots. Conventional impedance islanding detection relies on a sudden amplitude transition. This strategy fails if the power supplied by the micro grid system and the power needed by the load are not adequately matched. Micro grids are subsystems of distribution networks and are inherently unstable. Disconnecting a micro grid from the main grid while using inverters and rotation-based DGs causes' voltage, current, and impedance sequence components to shift. From equation (2) voltage and current for a positive, negative and impedance sequence can be expressed as in equation (6-9)

$$V_a^2 = \frac{1}{3}(V_a + a^2 V_b + aV_c) \tag{6}$$

$$I_a^2 = \frac{1}{3}(I_a + a^2 I_b + aI_c) \tag{7}$$

Negative sequence impedance as

$$Z_2 = \frac{V_a^2}{I_a^2} \tag{8}$$

Similarly positive sequence impedance as:

$$Z_1 = \frac{V_a^1}{I_a^1} \tag{9}$$

The sum of positive and negative sequence impedance as Z_{norm} in equation (10).

$$Z_{norm} = Z_1 + Z_2 \tag{10}$$

The resultant impedance sequence component is calculated from the absolute output of the difference measured (Z_{inst}) and normal Impedances (Z_{norm}) at the PCC in eq (11).

$$RSIC = \left|(Z_{norm}) - (Z_{inst})\right| \tag{11}$$

Where Z_{inst} is the sum of instantaneous impedances of positive and negative sequence components.

The identification of islanding is assumed to be faster and more accurate using a system that can differentiate between islanding and non-islanding scenarios. For this reason, the suggested detection method makes use of both positive and negative sequence impedance components. The three-phase voltages and currents at the PCC (node 650) are analyzed to determine their values.

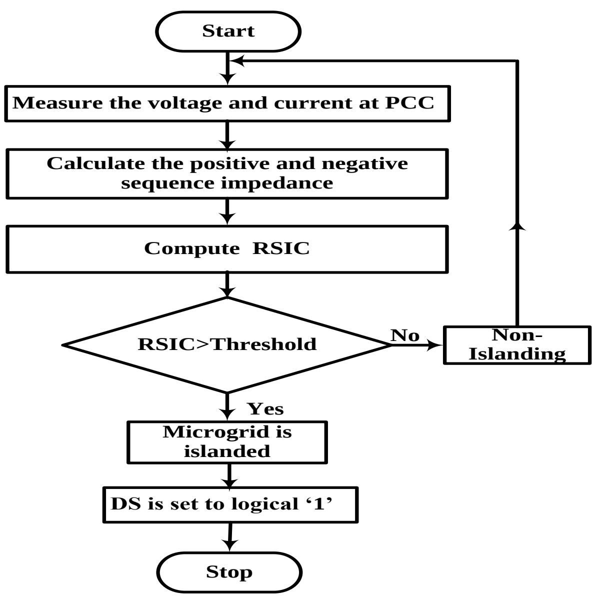


Fig. 2. Flow chart for the proposed detection technique.

To acquire the output, we fed the collected signals into a Sequence Analyzer and used equation (11) to calculate the absolute difference in impedance sequence component between the measured output and grid-connected instances as RSIC. A constant value can be obtained by calculating the mean and then comparing it to the threshold. The IDW is set to logical 1 by the timer if the mean of the RISC takes longer than the threshold. Whenever the non-islanding, measured RISC mean falls below the threshold, the IDW remains in the logical '0' state. The proposed algorithm is depicted in block diagram form in Fig.2.

2.3 Load Shedding (LS)

Island management is difficult because of the imbalance of power on the island. Load Shedding is used as a corrective mechanism in most of the current control schemes to keep the island running smoothly. A priority-based load-shedding strategy is developed to keep the power balance in the discovered island. When the island's power demand rises above the supply from the island's DG sources, the proposed load shedding process begins. Changes in frequency and voltage over time are used to rank the loads. The bus with the largest voltage and frequency swings is the greatest candidate for load shedding. Because the frequency and voltage fluctuations at the DG bus are not as severe as they would be without DG, the DG bus does not need to take part in the load shedding. All the other buses are ranked, and the loads are shed, until the system frequency and voltage of the buses are once again within threshold limits. Equation 12 expresses the overall amount of load shed in the system based on the rank and loads in the individual buses:

$$LS = PC_k * P_{load,k} \tag{12}$$

PC is the Parity Coefficient for a given bus, and it is found using Eq. 13 when $P_{load,k}$ is the load on bus '*k*'.

$$PC = D_k * \beta_f * \beta_v \tag{13}$$

Where β_f and β_v are the frequency and voltage aspects of the buses, computed using equations (14) and (15)

$$\beta_f = \frac{f_{k,t}}{f_{\text{int},0}} \tag{14}$$

$$\beta_v = \frac{V_{k,t}}{V_{\text{int},0}} \tag{15}$$

when load shedding is commenced, the frequency at bus '*k*' is $f_{k,t}$ and when islanding is identified, the initial frequency at bus is $f_{\text{int},0}$. Bus '*k*' voltage $v_{k,t}$ is measured when load shedding begins; bus 'initial' voltage $v_{\text{int},0}$ is measured when islanding is identified. Each bus's load shedding in a distribution system is an on-off, hence D_k is always either 0 or 1. The reliability of the isolated system is measured both before and after load shedding to determine the efficacy of the proposed priority based load shedding technique. The reliability analysis makes use of conventional reliability indices, line failure rates, and repair times. Reliability indices are commonly used, with SAIDI, SAIFI, CAIDI, ENS, and AENS being some of the most well-known. Client failure notifications are a common source for these metrics [20]. The quantitative reliability study of the system measures the effect of the intended load shedding scheme. Standard reliability indices such as SAIDI, SAIFI, CAIDI, ENS, and AENS are used both before and after the load shedding process to assess the performance of the proposed load shedding scheme.

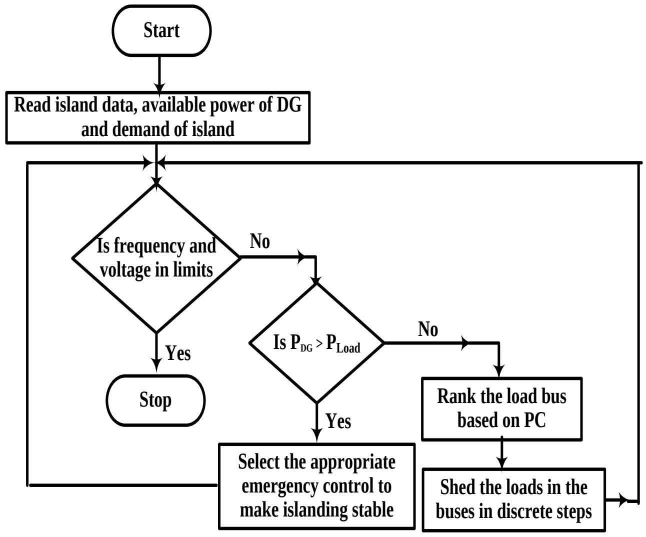


Fig. 3. Flowchart of Proposed Priority Based Load Shedding method.

Since this research is based on the number of affected consumers, the effect of emergency load shedding systems can be quantified using traditional reliability indices. Reliability indicators for the power shedding scheme also list affected consumers. For a visual representation of the priority based load shedding technique presented in [26], see Figure 3.

3. Results and Discussion

Numerous islanding and non-islanding events were examined to validate the efficacy of the suggested detection method. This section provides a comprehensive enumeration of various simulated occurrences and the corresponding number of simulated examples for each event. The findings are briefly stated as follows.

3.1 Islanding (IS)Cases

3.1.1 Variation in Load Quality Factor

Load quality (Q.F) factors between 1 and 2.5 are evaluated for islanding detection in accordance with IEEE standards. The results of RSIC with a varying load quality factor and no power mismatch are displayed in Fig. 4(a). The magnitude difference between grid-connected and islanding RSIC can be reduced by raising the load quality factor. A higher Q.F indicates a higher load of reactance, which reduces the frequency of oscillations in the voltage and current waveforms following islanding. The ISDW reveals a phenomenon analogous to island life in all its forms. In this work, the load quality factor for islanding scenarios is set at 2.5 and for non-islanding scenarios it is set at 1.0. The trigger signal was depicted in Fig. 4(b). The suggested approach guarantees reliable islanding detection even at the extremes of the typical load quality factor.

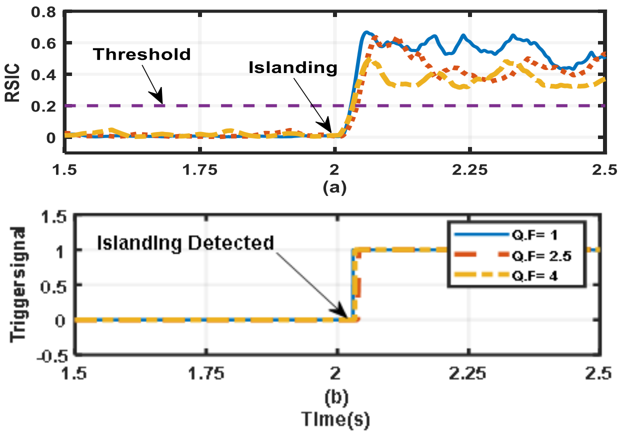


Fig.4. (a) RSIC for the impact of varying quality-factor (b) Trigger signal.

3.1.2 Imbalance in Real Power

Real power imbalances between the D.G. power and the load power were shown by the RSIC variations in Fig. 5(a). When the breaker opens at 2 second, the RSIE amplitude is larger than the initial value. . If the real power discrepancy is positive, the D.G. power will be higher than the load power, and vice versa if the mismatch is negative. Cases where real power is increased or decreased by 2% to 20% are explored. If there is more than a 20% difference in power use, the voltage levels are outside the NDZ. That's why we've settled on a value of 20% for the greatest possible power disparity. The trigger signal was depicted in Fig. 5(b).

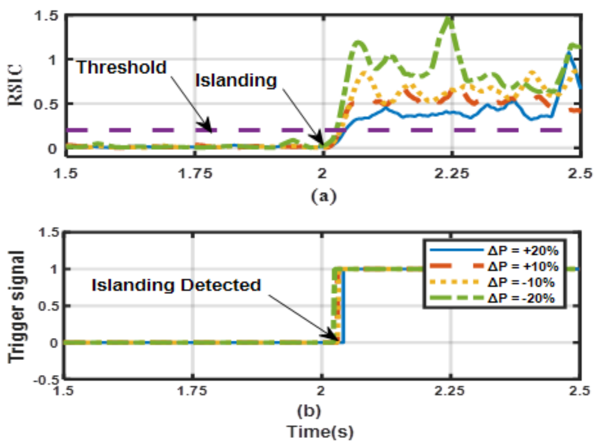


Fig.5. (a) RSIC for the impact of varying real power (b) Trigger signal.

3.1.3 Imbalance in Reactive Power

RSIC signal for reactive power imbalance for inductive and capacitive-load is shown in Fig.6 (a), respectively. When the breaker opens at 2.0 seconds, the detecting signal RSIC amplitude is larger than the threshold level. In this way, the islanding condition is recognized by the algorithm. Consider the case of a positive reactive power mismatch, in which the capacitive demand is lower than the inductive and the inductive demand is higher than the capacitive. The range of reactive power variances from 0.2% to 2% is considered to analyze both increases and decreases in reactive power. When the reactive power imbalance is greater than the +2% and -2% thresholds, islanding is identified and the frequency deviates from the NDZ . The trigger signal was depicted in Fig. 6(b).

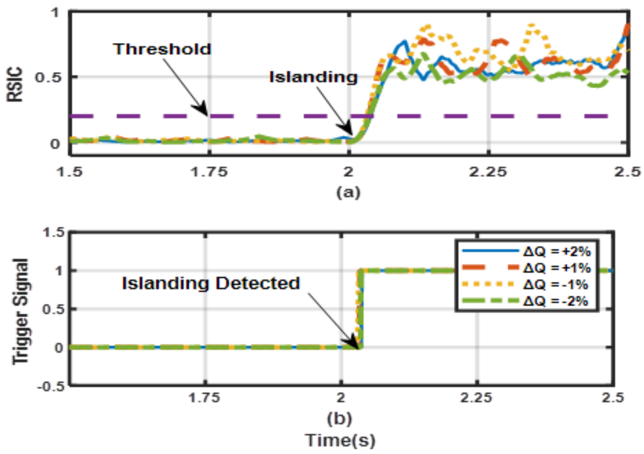


Fig.6. (a) RSIC for the impact of varying reactive power (b) Trigger signal.

3.2 Non-islanding Cases

Significant factors contributing to non-islanding include capacitance, load switching, and short-circuit faults. This section presents a thorough categorization of different simulated Non-islanding scenarios. The results are concisely summarized as follows.

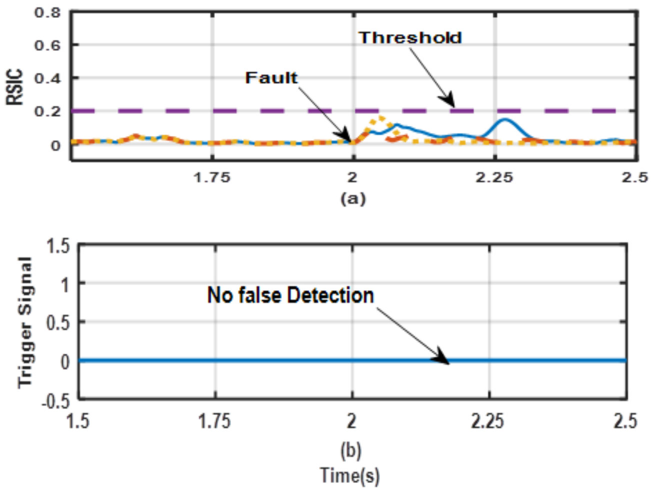


Fig.7. (a) RSIC for the short circuit faults (b) Trigger signal.

3.2.1 Short Circuit Faults

Simulations of three-phase faults (LLL), two-phase faults (L.L.), and phase-ground faults (L.G) are all possible. When the circuit breaker in the parallel feeder trips, the fault gets fixed in less than two seconds. In each scenario, the fault resistance is adjusted between 1 and 75 ohm. Fig.7 (a) depicts the RSIC fault-detection signal for LLL, L.L., and L.G. faults. Fig.7(b) shows that the detection signal magnitude was below the threshold for all fault categories, indicating that no false detections occurred.

3.2.2 Capacitor Switching

At 2.0 seconds, the capacitor bank turns on, and it goes from 10% to 100% in steps that last 0.02 seconds each. With the same 0.02-second interval between each step, the capacitor banks are discharged from 100% to 10% after 2.5 seconds. Figure 8(a) depicts the islanding detection signal for 100% capacitor bank switching. As demonstrated in Fig. 8(b), a false trip can be avoided by using a suitable threshold, as the peak in these switching circumstances quickly saturates and has a value below the threshold.

3.2.3 Load Switching

In this scenario, we think about turning loads on and off. At 2.0 s, the load is activated, and from there it is gradually increased in 10% increments up to 100%, with each increment lasting 0.02 s; starting at 2.5 s, the load is gradually decreased from 100% down to 10%, also in 10% increments. For full load switching, the islanding detection signal RSIC is displayed in Fig. 9(a). Since the RSIC signal is flat throughout load switching, the detection signal returned to normal values less than the threshold, preventing an incorrect islanding detection (Fig.9 (b)).

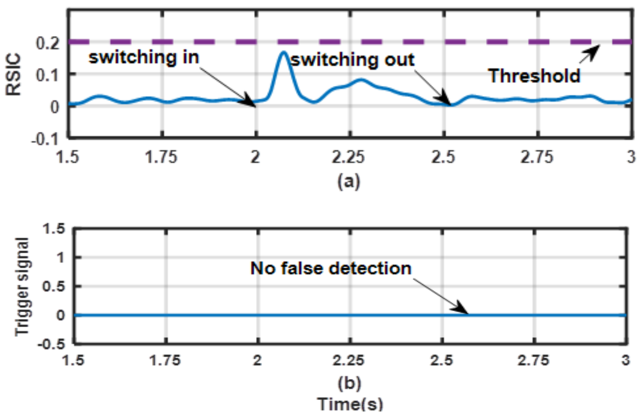
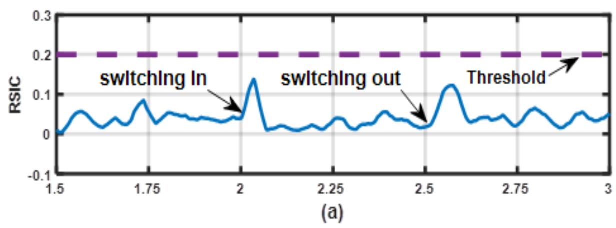


Fig.8. (a) RSIC for the 100% capacitor bank switching (b) Trigger signal.



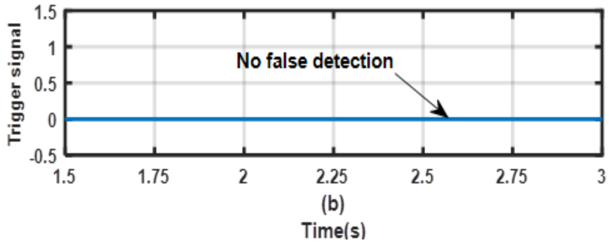


Fig.9. (a) RSIC for the 100% load switching (b) Trigger signal.

3.3 Load Shedding

Before and following load shedding using the suggested priority-based strategy for the 13 Bus system, the voltage and frequency parameters of the islanded bus are depicted in Figures 10(a) and (b), accordingly. Islanding occurs at 0.3 seconds and load shedding algorithm starts at 0.5 seconds it makes the system Voltage and frequency stable at 0.8 seconds. In Table 1, the load-shedding order for the priority-based load-shedding is shown.

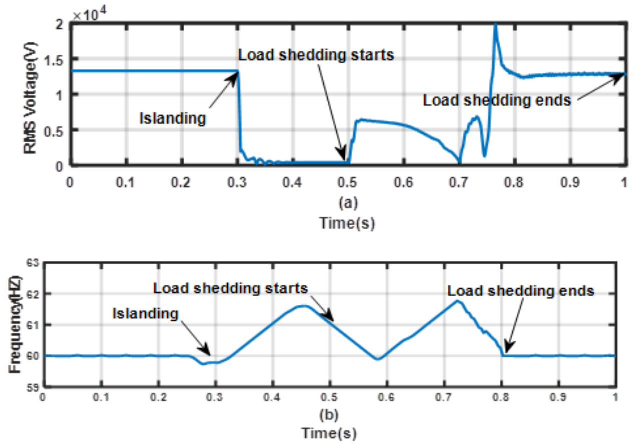


Fig.10. (a) RMS voltage (b) Frequency for load shedding.

Table-1: PC-based demonstration of load ranking.

Load Ranking	Load Number	Load Demand (kVA)	Type of load
1	5	420+ j200	Heavy load
2	8	400+ j200	Heavy load
3	7	310+ j1600	Heavy load
4	4	300+ j160	Heavy load
5	9	130+ j90	Heavy load
6	1	75+ j40	Light load
7	11	75+ j35	Light load
8	10	75+ j30	Light load
9	6	60+ j35	Light load
10	2	60+ j30	Light load
11	12	60+ j25	Light load
12	3	40+ j25	Light load

4. Discussion with Literature

This section compares the Islanding detection times of the proposed method for different quality factors (Q.F) to the detection times, NDZ measurements, and load shedding described in the literature. As shown in Table 2, the islanding detection times for the suggested method are much shorter than those of a few earlier research works.

TABLE 2. Comparison to the literature

Reference	Q.F	Detection Time (ms)	NDZ	Need of Time Delay	Load Shedding
[6]	1	>340	Small	Yes	No
[20]	1	>300	Small	Yes	No
[27]	2.5	<350	Small	No	No
[28]	0.96	<454	Small	No	No
[7]	2.5	>325	Small	Yes	No
[29]	2.5	>315	Small	Yes	No
[30]	2.5	>200	Medium	No	No
[31]	2.5	>350	Small	No	No
Proposed	1	31.2	Zero	No	Yes
	1.5	32.6			
	2	34.5			
	4	32.2			

5. Conclusion

This study introduces a new method for detecting passive islanding, which involves measuring voltage and currents at the PCC and utilizing the resultant sequence impedance components. Employing the methodology as mentioned above, islanding was identified within an approximate time frame of 30 milliseconds. Several island-based scenarios were used to test the effectiveness of the proposed processes. The proposed procedures effectively differentiate between islanding and non-islanding situations with 100% accuracy rate. Further, it is observed that the proposed method is faster than the existing methodologies in the literature owing to its low computational time. These approaches can also determine the most optimal feasible threshold value, even if RSIC varies for causes other than islanding. An adjustable PC parameter is employed to decide which buses will be affected by the island's proposed priority-based load-shedding scheme. The proposed technique offers a more efficient approach to mitigating load shedding in order to restore frequency and voltage stability on the island, as compared to the conventional load shedding strategy. Before implementing load shedding, the suggested power control parameter considers the presence of DG units and the occurrence of frequency and voltage changes on a specific bus.

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