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Deep Belief Learning Network Based IC-DSTATCOM For PQ Analysis

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Abstract- The varieties of energy structures that afford large amounts of energy to the global power economy has led to a reduced quality in the power distribution network (PDN). Most traditional methods use direct coupled distributed static compensator (DC-DSTATCOM) which is dependent on specific line parameters. Hence, it performs poor adaptability to the PDN. Aim at enhancing power quality (PQ); this study focuses on the deep belief learning network (DBLN) controlled inductively coupled distributed static compensator (IC-DSTATCOM). Considering the system variation and impact, an individual DBLN structure is accumulated for each and every phase. The weight obtained from the DBLN mechanism is caused for reference currents generation. The filtering performance of the IC-DSTATCOM is revealed better by combining the effect of the transformer and DSTATCOM impedance. So, the IC-DSTATCOM is augmented with better dynamic performance with PQ abilities as compared to DC-DSTATCOM in terms of shunt compensation such as, THD reduction, power factor (p.f.) improvement, better voltage regulation and load balancing etc. The IEEE - 2030 - 7 - 2017 and IEC - 61000 - 1 grid code are used to evaluate the effectiveness as per the benchmark value using MATLAB/Simulink.

Keywords DBLN technique, DC-DSTATCOM, IC-DSTATCOM, PQ.

1. Introduction

Nowadays, all the governments throughout the globe are captivating the judgment for large-scale combination of renewable and non renewable resources to look up the energy footprints [1-5]. Various government, semi government, and non-government financial supports are provided for the installation of improved versions of custom power devices (CPD). Among the various forms of CPDs, distributed static compensator (DSTATCOM) is best CPDs for shunt compensation in the power distribution network (PDN) [6-10]. This is achieved due to flexible, silent, less maintenance cost, extended capability and easier for real time implementation [11-13]

1.1 Review of Literature and Research Background

To keep up a protected, efficient and reliable function of the PDN, the source voltage (v_s) should be within 0.95≤ v_s≤1.05 whereas the source current (i_s) be required to be less than the grid code limits. The foremost problems in the PDN are the current related PQ issues due to uncertainty in load demand and mismatch in between the impedance parameters among the devices [14-16]. PDNs are intrinsically unbalanced due to the above said causes which furthermore causes higher system loss. Hence, it becomes essential to develop a machine learning algorithm supported by DSTATCOM for unbalanced PDN to maximize the system benefits [17-19].

In many of the previous research articles, DC-DSTATCOM is presented for the shunt compensation [20-22]. But, some severities occur at the common point or point of common coupling (PCC) due to the DC- DSTATCOM, source and load such as flow of short circuit current, poor protection, and some thermal losses.

Due to these above said drawbacks of DC-DSTATCOM, nowadays the development was started on the area of IC-DSTATCOM [23-24]. It is obtained by connecting the non-linear loads to the source through a coupling transformer. The influence of the inductive transformer permits the inductance balancing in the PDN to analyze the system stability [23]. Moreover, it provides robustness against the load variation over a wide range. Also, it bears a number of merits such as less switching stress, flexibility, controllability, improved balance voltage at PCC, increasing the compensation capability, and different combinations are possible. To analyze the problems involved in power and energy, different types of non adaptive and adaptive control algorithms are employed [25-28]. However, some of the shortcomings such as premature convergence and solutions are not suitable for a competent planning framework (CPF). The prime objectives such as better voltage regulation at PCC, harmonics reduction, power factor (p.f.) improvement and load balancing are considered. For designing the CPF, unsupervised machine learning technique is required [29-32]. This algorithm is a significant machine learning move that seeks to learn an optimal strategy based on the feedback from the environment computed by a reward function [33].

1.2 Novelty and Contribution

In order to achieve a CPF, IC-DSTATCOM is incorporated for unbalanced PDN to improve the shunt compensation.

The major contributions are mortified in this way:

(i) Inductive transformer is deployed in the DSTATCOM as a perfect matching impedance device for nonlinear systems, which is also an integral part of controlling the shunt compensation as per acceptable limits.

(ii) The DBLN algorithm is deployed to improve the PQ solution and reduce the computational complexities.

(iii) The significant harmonics reduction and p.f improvement are achieved.

(iv) The proper voltage regulation and voltage balancing are ensured due to the proposed device.

(v) The IC-DSTATCOM with DBLN control technique enhances the operating capacity during unbalanced load, which further increases the flexibility of the PDN. Hence, the reliability of the PDN increased.

(vi) The suggested topology with DBLN control technique quantitatively compares with other published research work under PQ issues and their different parameters values are presented in Table 3.

2. Overview of PQ Assessment

The computer business equipment and manufacturing association (CBEMA) assessment is surveyed by the Electric power Research Institute (EPRI), National Power Laboratory (NPL) and Canadian Electrical Association (CEA). Reviewing the assessment, the cause and effect of faults and loading are considered in this study. The details of the tolerance and intolerance events are exposed in the Fig.1. To reach this level of coverage of PQ solution, DBLN based inductively coupled DSTATCOM is analyzed.

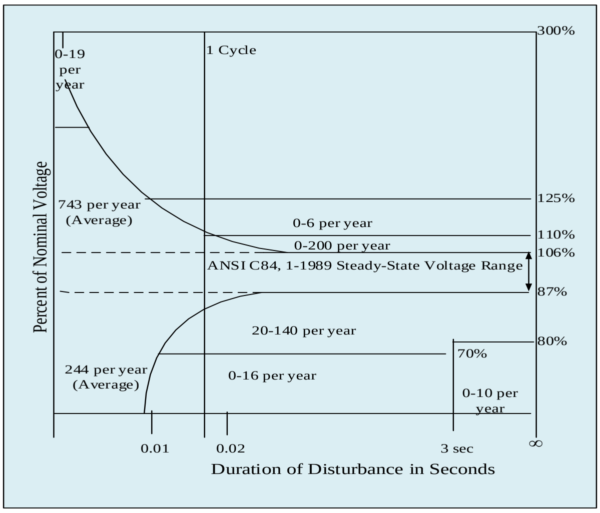

Fig.1.CBEMA curves for PDN faults versus voltage and duration

3. Circuit Description of The DSTATCOM

The traditional PDN consists of stable three phase source with uncontrolled rectifier with R (resistance) and L (inductance) as a non linear load. Whereas the both DC-DSTATCOM and IC-DSTATCOM is attached at the PCC of PDN. The traditional DSTATCOM, PDN with DC DSTATCOM and PDN with IC-DSTATCOM are presented in Fig. 2, Fig. 3 and Fig. 4 respectively.

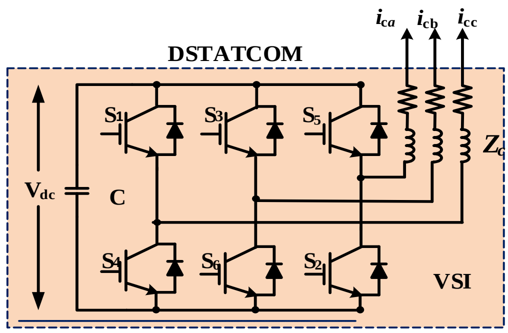

Fig.2. Traditional DSTATCOM (2-level VSI)

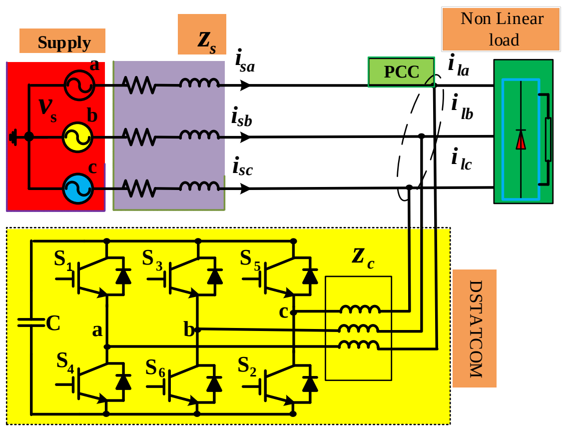

Fig.3. PDN with DC- DSTATCOM

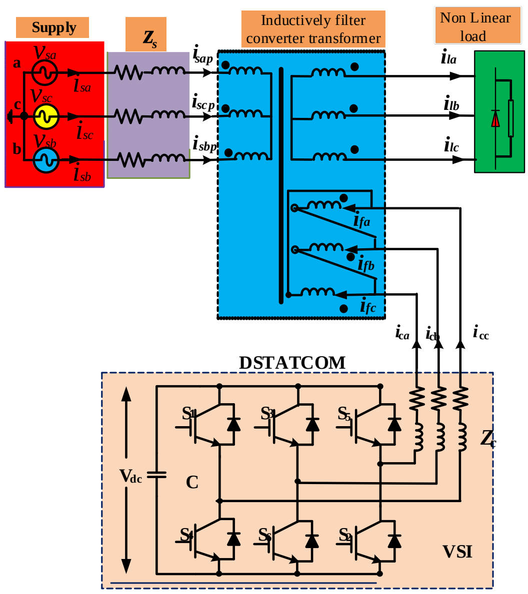

Fig.4.PDN with IC- DSTATCOM

The switching pulses of both compensators are generated by using DBLN algorithm. The design of two level (6-pulses) based DSTATCOM are shown in Fig.3 and 4. The primary, load and filtering currents are $i_{p,}i_l$ & i_f correspondingly. The Z_c is denoted by the compensator impedance.

3.1 Modeling and Designing of Inductive Transformer

The proposed IC-DSTATCOM configures inductively filter converting transformer (IFCT) topology built by three windings as shown in Fig. 4. The star connected primary windings are connected with the PDN, star connected secondary windings are connected with load and delta connected filtering winding is connected with DSTATCOM. The unique IFCT provides better voltage regulation at the PCC of the proposed system. Here, N_1, N_2 and N_3 are three turns of the IFCT, $Z_p$is the primary winding impedance, Z_s is the series impedance and Z_g is the line impedance. So, $Z_g = Z_s+Z_p$. But Z_o is the filter side winding impedance, Z_c is the compensator impedance and Z_f is the tertiary winding impedance. So, $Z_g = Z_c+Z_f$.
The voltage balance equation of PW, SW and FW can be expressed as,

$$\begin{cases} N_1 i_{sap} + N_2 i_{las} + N_3 i_{caf} = 0 \\ N_1 i_{sbp} + N_2 i_{lbs} + N_3 i_{cbf} = 0 \\ N_1 i_{scp} + N_2 i_{lcs} + N_3 i_{ccf} = 0 \end{cases} \tag{1}$$

According to Kirchhoff's current law (KCL), the current equations in the primary side of the IFCT are written as

$$\begin{cases} i_{sap} = (v_{sa} - v_{sapo})/Z_{sa} \\ i_{sbp} = (v_{sb} - v_{sbpo})/Z_{sb} \\ i_{scp} = (v_{sc} - v_{scpo})/Z_{sc} \end{cases} \tag{2}$$

According to KCL, the current equations in the secondary side of the IFCT (load side) are written as

$$\begin{cases} i_{la} = i_{las} + i_{caf} \\ i_{lb} = i_{lbs} + i_{cbf} \\ i_{lc} = i_{lcs} + i_{cbf} \end{cases} \tag{3}$$

The current balance equations are shown below:

$$\begin{cases} i_{sap} + i_{sbp} + i_{scp} = 0 \\ i_{las} + i_{lbs} + i_{lcs} = 0 \\ i_{caf} + i_{cbf} + i_{ccf} = 0 \end{cases} \tag{4}$$

The total compensating current equations at filter side are written as

$$\begin{cases} i_{caf} = i_{ca} + i_{fa} \\ i_{cbf} = i_{cb} + i_{fb} \\ i_{ccf} = i_{cc} + i_{fc} \end{cases} \tag{5}$$

4. DBLN Algorithm

Having three input layers, three computational layers are Boltzmann Machine to generate latent featured and vector encoded weights, and three output layers are provided for conditional probability density function (CPDF) oriented updated weight [29-33]. The block diagram of DBLN control technique is presented in Fig.5. Here, j is considered as the neurons in the hidden layer and 'i'is the neurons in the computational layer.

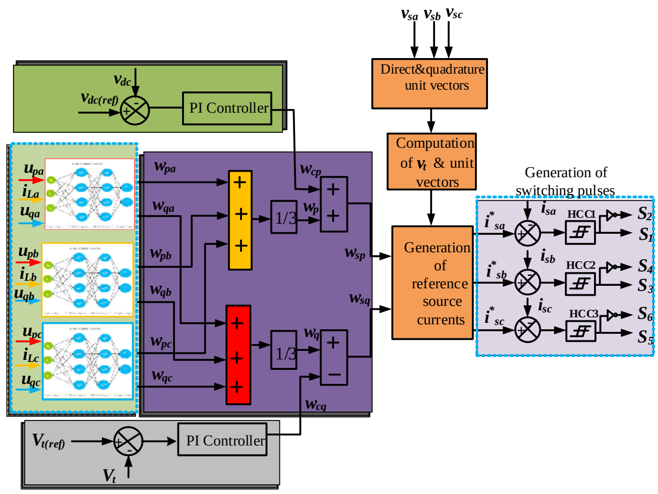

Fig.5. Block diagram of DBLN control technique

The active component of load current (w_{pa}, w_{pb}, w_{pc}) is computed using DBLN algorithm as follows:

$$W_{qa}^n = \sigma \sum_k W_{qa}^i h_k^{i-1} u_{pa}(n)(i_{la}(n) - w_{qa}(n-1) + b_j^i w_{qa}(n-1) \tag{6}$$

$$W_{qb}^n = \sigma \sum_k W_{qb}^i h_k^{i-1} u_{pa}(n)(i_{la}(n) - w_{qb}(n-1) + b_j^i w_{qb}(n-1) \tag{7}$$

$$W_{qc}^{n} = \sigma \sum_{k} W_{qc}^{i}\, h_{k}^{i-1} u_{pa}(n)(i_{la}(n) - w_{qa}(n-1) + b_{j}^{i} w_{qc}(n-1) \quad (8)$$

The "w_{pa}, w_{pb}, w_{pc}" reactive component of load current are computed using DBLN algorithm as follows:

$$W_{pa}^{n} = \sigma \sum_{k} W_{pa}^{n-1}\, h_{k}^{i-1} u_{pa}(n)(i_{la}(n) - w_{pa}(n-1) + b_{j}^{i} w_{pa}(n-1) \quad (9)$$

$$W_{pb}^{n} = \sigma \sum_{k} W_{pb}^{i}\, h_{k}^{i-1} u_{pa}(n)(i_{la}(n) - w_{pb}(n-1) + b_{j}^{i} w_{pb}(n-1) \quad (10)$$

$$W_{pc}^{n} = \sigma \sum_{k} W_{pc}^{i}\, h_{k}^{i-1} u_{pa}(n)(i_{la}(n) - w_{pc}(n-1) + b_{j}^{i} w_{pc}(n-1) \quad (11)$$

Similarly, considering the a, b and c-phase weighting factor, the reactive average value can be expressed as

$$w_a = \frac{w_{pa} + w_{pb} + w_{pc}}{3} \quad (12)$$

Similarly, considering the a, b and c-phase weighting factor, the reactive average value can be expressed as

$$w_r = \frac{w_{qa} + w_{qb} + w_{qc}}{3} \quad (13)$$

The "u_{pa}, u_{pb}, u_{pc}" are the unit voltage templates expressed as follows

$$u_{pa} = \frac{v_{sa}}{v_t}, u_{pb} = \frac{v_{sb}}{v_t}, u_{pc} = \frac{v_{sc}}{v_t} \quad (14)$$

By using quadrature unit voltage templates (u_{qa}, u_{qb}, u_{qc}) are calculated as

$$u_{qa} = \frac{u_{pb} + u_{pc}}{\sqrt{3}}, u_{qb} = \frac{3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}}, u_{qc} = \frac{-3u_{pa} + u_{pb} - u_{pc}}{2\sqrt{3}} \quad (15)$$

Where, v_t can be expressed as

$$v_t = \sqrt{\frac{2(v_{sa}^2 + v_{sb}^2 + v_{sc}^2)}{3}} \quad (16)$$

The error in dc voltage "v_{de}" can be expressed as

$$v_{de} = v_{dc\,(ref)} - v_{dc} \quad (17)$$

The Proportional-Integral (PI) controller processes the v_{de}signal for controlling the constant dc bus voltage which can be expressed as

$$w_{cp} = k_{pa} v_{de} + k_{ia} \int v_{de} dt \quad (18)$$

The "w_{sp}" is the total active component, expressed as follows

$$w_{sp} = w_a + w_{cp} \quad (19)$$

The error in ac voltage (v_{te}) can be expressed as

$$v_{te} = v_{t\,(ref)} - v_t \quad (20)$$

The Proportional-Integral (PI) controller processes the v_{te} signal for controlling the constant ac bus voltage which can be expressed as

$$w_{cq} = k_{pr} v_{te} + k_{ir} \int v_{te} dt \quad (21)$$

The "w_{sq}" is the total reactive component, expressed as follows

$$w_{sq} = w_r - w_{cq} \quad (22)$$

The "i_{aa}, i_{ab}, i_{ac}" are the instantaneous reference source active component, expressed as follows

$$i_{aa} = w_{sp} u_{pa}, i_{ab} = w_{sp} u_{pb}, i_{ac} = w_{sp} u_{pc} \quad (23)$$

Similarly, the "i_{ra}, i_{rb}, i_{rc}" are the instantaneous reference source reactive component, expressed as follows

$$i_{ra} = w_{sq} u_{qa}, i_{rb} = w_{sq} u_{qb}, i_{rc} = w_{sq} u_{qc} \quad (24)$$

Finally, the "$i_{sa}^*, i_{sb}^*, i_{sc}^*$" are the reference source currents, expressed as follows

$$i_{sa}^* = i_{aa} + i_{ra}, i_{sb}^* = i_{ab} + i_{rb}, i_{sc}^* = i_{ac} + i_{rc} \quad (25)$$

At the end, the error found from "i_{sa}, i_{sb}, i_{sc}"*and* "$i_{sa}^*, i_{sb}^*, i_{sc}^*$" by comparing are fed to a Hysteresis current controller (HCC).

5. Simulation Results Using MATLAB

5.1 Simulation Results of DC-DSTATCOM

The simulation study of the DC-DSTATCOM in PDN is analysed to show the effectiveness and feasibility in the Fig. 5.1. The system Simulation parameters are arranged in Table 1. In this Fig. 5.1, all the subplots are source voltage and source current, source current, source voltage and load current, compensating current, DC-link voltage are arranged in the order of top to bottom wise.

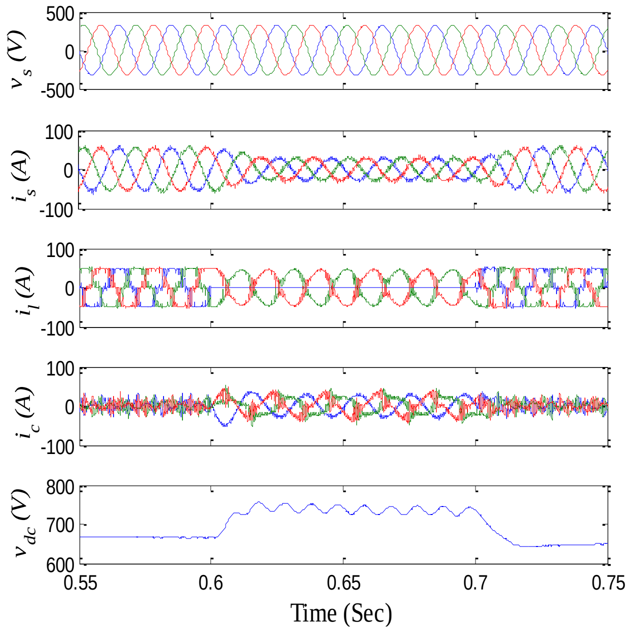

Fig. 5.1 Results shown from (lower part of the waveform to upper); Inverter DC-link voltage, 3-phase compensating current, 3-phase non-linear load currents, 3-phase source currents and stable 3-phase supply voltage

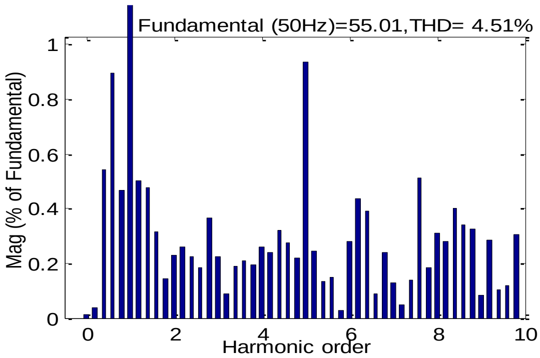

Fig. 5. 2. Source current THD with DC- DSTATCOM

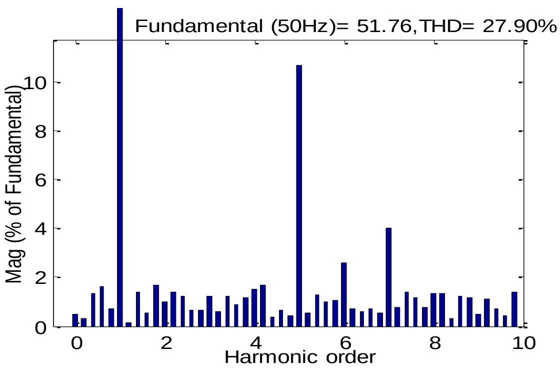

Fig. 5. 3. Load current THD with DC- DSTATCOM

When the DC-DSTATCOM switched on, it was noticed that the p.f. of the system improved to 0.94 and source current THD% of the system decreased to 4.51% shown in Fig. 5.2. The load current THD% 27.90 is shown in Fig.5.3. To check the effectiveness of the system, DC-DSTATCOM is testified under both balanced and unbalanced loading scenarios. Unbalanced loading is created by disconnecting the phase ‘a’ load between 0.6 Sec to 0.7 Sec. During this interval, phase ‘a’ load current is zero. Furthermore, the DC link voltage is governed with an acceptable voltage regulation of 671.6V under this observation.

5.2 Simulation Results of IC-DSTATCOM

The simulation study of the IC-DSTATCOM in PDN is analyzed to show the effectiveness and feasibility in the Fig. 6.1. When the IC-DSTATCOM switched on, it was noticed that the p.f. of the system improved to 0.99 and source current THD% of the system decreased to 3.57% shown in Fig. 6.2.The load current THD% 27.90 is shown in Fig.6.3.

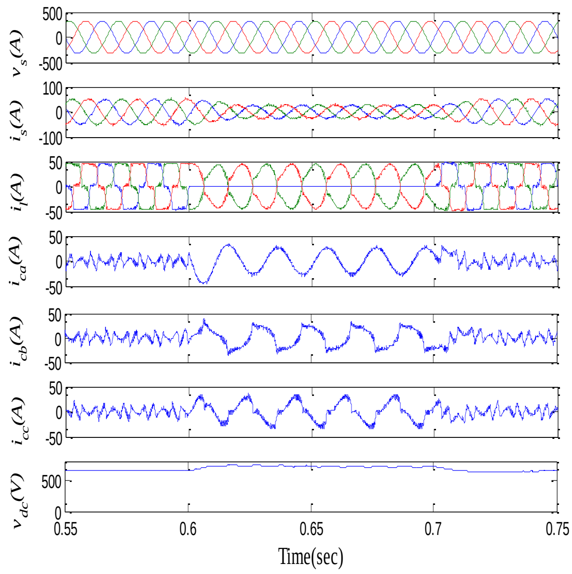

Fig.6.1. Results shown from (lower part of the waveform to upper); Inverter DC-link voltage, 3-phase compensating current, 3-phase non-linear load currents, 3-phase source currents and stable 3-phase supply voltage

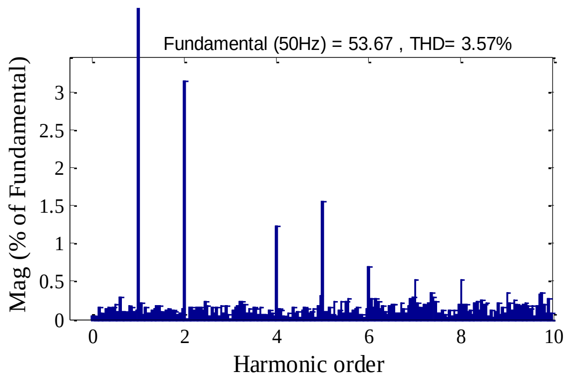

Fig.6.2. Source current THD with IC-DSTATCOM

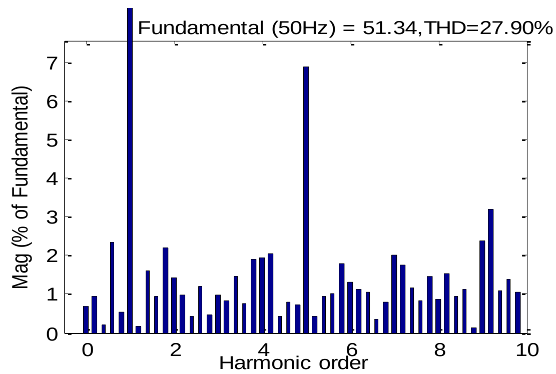

Fig.6. 3 Load current THD with IC-DSTATCOM

Furthermore, the DC link voltage is governed with an acceptable voltage regulation of 605.6V under this observation. Hence, the system performs justifiable PQ improvement as per IEEE519-2017 grid code and ensures better power.

Table 1.System parameters

Symbol	**Definition**	**Value**
v_s	3- phase source voltage	230V/phase
f_s	Frequency	50Hz
R_s	Source resistance	0.5Ω
L_s	Source inductance	2mH
K_{pr}	AC Proportional controller	0.2
K_{ir}	AC Integral controller	1.1
v_{dc}	DC link voltage	600V
C_{dc}	Capacitor	2000μF
K_{pa}	DC Proportional controller	0.01
K_{ia}	DC Integral controller	0.05
R_c	VSC resistance	0.25Ω
L_c	VSC inductance	1.5mH

In order to have uniform and balanced supply current for future load, DSTATCOM will inject more compensator current to maintain the reactive power at the PCC.Hence, rising in DC link capacitor is obvious for maintaining better voltage regulation of PDN. Unbalanced loading is created by disconnecting the phase 'a' load between 0.6 Sec to 0.7 Sec. The fluctuation in DC link voltage of IC-DC-DSTATCOM during balanced loading condition, DSTATCOM inject the compensator current supplies to meet the actual reactive power at the point of common coupling (PCC). Hence, the topology possesses its own control action in regulating the DC-link voltage during this loading conditions. But in unbalanced loading condition, phase 'a' load current is zero. Comparative anlysis of DC-DSTATCOM and IC-DSTATCOM under PQ issues are arranged in Table 2.

Table 2. Performance parameters

Performance parameter	DC-DSTATCOM	IC-DSTATCOM
i_s(A), %THD	55.01, 4.51	53.67, 3.57
v_s (V), %THD	321.4, 2.23	321, 1.42
i_l (A), %THD	51.76, 27.90	51.34, 27.90
p.f.	0.94	0.99
v_{dc} (V)	671.6	605.6

Table 3: Comparisons of DBLN algorithm with other published work

Under PQ issues	Source current (THD%)	Load Current (THD%)	P.F
DBLN Algorithm	3.57	27.9	0.9
Reference [10]	4.14	27.9	0.9

6. Conclusion

This paper proposed a design and implementation aspect of DBLN algorithm for the IC-DSTATCOM under uncertainties of PDN loading. It can be concluded that:

- The balanced, sinusoidal, distortion-free source current is achieved with improved p.f. at source side.
- The %THD has reduced significantly after compensation as per IEEE grid code (IEEE 519-2017) and IEC grid code (IEC 61000-3-12). The allowable variation in dc-link voltage causes minimum voltage stress across the semiconductor switches. Hence semiconductor switching losses are reduced to an enormous level which further increase the service period and efficiency of proposed IC-DSTATCOM.

Therefore, it has proven to be a more efficient method for PQ solution in the PDN.

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