# Design and Implementation of a Novel Zeta Converter for DC Bus Voltage Regulation

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**Abstract-** This paper proposes a Novel Zeta Converter (NZC) with high voltage gain to regulate the voltage in the DC bus. The proposed topology is developed with the inclusion of additional capacitor in the conventional zeta converter to improve the voltage gain. This structure reduces the number of switching devices and losses when compared with the conventional DC-DC high gain converters with higher efficiency. The converter is demonstrated in conjunction with a photovoltaic (PV) system to maximise the output voltage of the PV system and eminent P & O algorithm based Maximum Power Point Tracking (MPPT) has been employed. The proposed system yields a constant output voltage for 13% of load variation. A comparison is made between the proposed system with conventional topology and it is inferred that the output voltage can be made constant with minimum number of components and reduced losses. A simulation is carried out in MATLAB/Simulink and validated in real time with dsPIC microcontroller. The simulation results are in line with the hardware result.

**Keywords** Modified zeta converter, MPPT, P&O algorithm, Photovoltaic system, voltage regulation.

## 1. Introduction

Electricity is critical to our daily lives, and generation from fossil fuels will be available for a finite period of time only as resources deplete. Renewable energy sources are used to generate electricity in order to meet the load demand [1],[2]. Natural resources could be used to offset energy demand. This converts solar energy into electrical energy which is connected to the grid using PV arrays. However, PV array offers a better result, but there exists an extremely lower output voltage. As a result, power electronic modules were used to vary the output voltage. Certain types of boost power circuits are capable of regulating the output voltage [3]. Despite of this, it is not possible to increase the output voltage above a predetermined threshold [4]. Boost converters were commonly used to raise the devices voltage which are operating at a higher duty cycle ratio. However, overall efficiency is reduced as a result of switching loss as well as Equivalent Series Resistance (ESR) of the input impedance.

Zeta converters are employed to overcome these limitations, as they are a type of buck-boost converter. However, the gain of the system continues to fail due to switching losses and other components [5], [6]. Interleaved boost converters, coupled inductors structures, capacitor-based voltage multiplier are used to improve the voltage gain [7] However, each converter has a number of distinct pros and cons.

The primary shortcoming of a soft switching-based converter is circuit complex nature and increased component count. These converters [8] are operating in the mode of Zero

Voltage Switching (ZVS), which results in a decrease in switching losses and increases the efficiency. Voltage multipliers are integrated with converters to achieve high gain voltage. A voltage multiplier is a device that has constant voltage ratio. The primary benefit of utilizing those multipliers are lighter, smaller in size, have a higher power density, are more efficient, and have a less magnetic structure. The output voltage of the circuit cannot be regulated with this component arrangement because the circuit is primarily dependent on the input voltage [9]. Additionally, it increases the semiconductor switches, which raises the cost and increases the size of the system. This is reflected in the fact that photovoltaic systems do not employ MPPT .

Recently, variety of voltage multiplier topologies have been proposed, resulting in the use of more capacitors and controllers [10]. The system possesses n number of capacitors and 2n number of switches in a voltage multiplier converter topology [11]. Those topology uses multilevel flying capacitor-based boost converter. $nV_{in}$ is the amount of DC voltage generated at the output for a given input voltage ($V_{in}$). It was noted that for increasing the output voltage, more number of power switches were required. Additionally, the output voltage is unregulated. Another voltage multiplier is developed with a switch count of 3n for n capacitors and an output voltage calculated as $(n+1)V_{in}$ [12]. This topology produces a discontinuous output current and an unregulated output voltage which is not preferred for PV applications. The major drawbacks of high gain in voltage [13] based converters include the following: Produces a discontinuity in the input current, the voltage at the output is difficult to regulate [14], not applicable for photovoltaic applications.

It is evident from the above literate that there is quest of proposing a novel high DC-DC converter with high voltage gain. This article describes a novel improved zeta converter possessing higher voltage gain for photovoltaic applications. This can compensate for the short comings [16],[17] of topologies proposed in the literature. Here, both simulation as well as experimental results were included to validate the proposed topology's characteristics. The primary drawback of conventional zeta converters is that: lower voltage gain and produces an intermittent current in the input which are overcome by the proposed methodology. The methodology without transformer, and N number of power converters are required whose control [18] signals are having 2π/N radians of phase shift. The structure discussed in gives the unregulated and unrectified [19] output voltage.

The proposed converter is designed to overcome the aforementioned disadvantages. It offers the following benefits: the design's gain has been increased, while the duty cycle is adjusted appropriately, it is possible to regulate electrical voltage, when used in photovoltaic applications, can track maximum power, provides cost savings, provides less loss due to the reduced switches, the suggested model generates a continuous current at the input. Highlights of the paper are

1. By proposing the modified novel zeta converter, a non-inverted output can be achieved which is essential for any DC power application.

2. In addition, the proposed system can use minimum number of components [20] like switches, diodes, and capacitors, which in turn reduces the cost, and size of the system when compared to available [21] methodologies especially for dynamic EV battery [22] charging [23] applications[24].

3. Added to that, the proposed system is capable of maintaining a constant output voltage even if the load is varied up to 13%. Another advantage of the proposed work is that it gives a higher [25] efficiency of about 94%. With likened methods.

4. This system is efficient and well suited for maintaining a constant voltage at DC bus. Also it can be well suited for injecting a constant voltage from a PV source or from a wind energy conversion systems to the load.

### *1.1 Maximum power point tracking (MPPT)*

In order to extract the maximum power output from any photovoltaic [26] panel can be achieved by incorporating a controller with MPPT. In general, there are two different approaches available by which the maximum power can be extracted. One of the approaches is direct technique and the other is indirect technique. Fixed voltage, short circuit current and open circuit voltage are falling under indirect approach. Here very simple assumptions and periodic estimation is incorporated which makes the approach easy. In the fixed voltage mode of approach, only the operating voltage can be altered under different irradiation levels so as to get larger MPP voltages. But the final output of this approach is not yielding a fruitful result because of seasonal changes like winter and summer with varying levels of irradiation and temperature. On the other side, the indirect technique[27] is open circuit voltage mode of approach. When compared to other mode of approaches, this is one of the simple and easiest way to get the maximum output voltage. The maximum output voltage can be achieved by multiplying the constant K with the open circuit voltage. But the value of K is made under assumption which gives reduction in the overall efficiency[28] as monotonously the value of open circuit voltage needs to be found with respect to change in the irradiation level.

Conversely, direct methods of MPP ensure swift response than indirect methods and P&O method is one among them.

### 1.2 P & O Algorithm

This most popular algorithm is created with the help of simple feedback arrangement and very less parameters. In this algorithm, the cell voltage is cyclically given a perturbation and the received output power is then to be compared with the former power. If the received power is increased then, the procedure is repeated else reversed. The increment and decrement of the output voltage is decided by the output power received from the cell. The operating point of the cell on the left side of the MPP shows an increase in voltage which leads output power and this condition shows that the perturbation is required towards the right to attain MPP. Conversely, perturbation is required towards the left to attain MPP. The flow chart of the P&O method is shown in the Fig 1

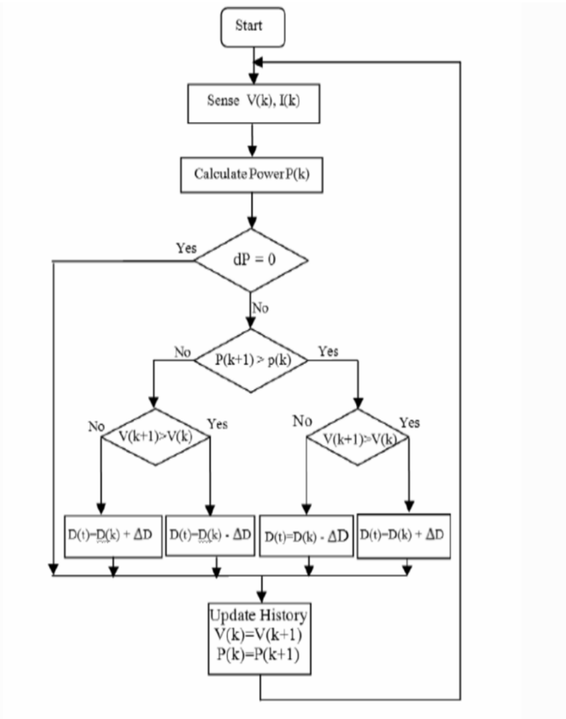


**Fig**.1. Flow chart of P&O method

## 2. Proposed Enhanced Zeta Converter

This paper contributes a modified novel zeta converter where the charge pump is effectively incorporated in the basic zeta circuit in such a way that the gain of the proposed system is predominantly increased. The proposed system utilises less number of components to achieve a greater voltage gain which when compared to the existing topologies of same structures. The circuit diagram of the proposed high zeta converter is illustrated in **Fig** 2. The converter is operated in dual stage mode, in which during the initial stage, a classic zeta converter is used, and during the next stage, a high gain boost power converter is used. $C_1$,$C_2$,$C_3$,$C_4$ and $C_5$ are charging capacitors and $T_1$, $T_2$,$T_3$ are switches where $T_1$ is the switch connected in the conventional zeta converter and switches $T_2$ and $T_3$ are the switches connected in the second stage of zeta converter. Moreover, diodes $D_1$ & $D_2$ are connected in the input stage and diodes $D_3$,$D_4$,$D_5$ &$D_6$ are connected in the second stage of the proposed structure. Two inductors $L_1$& $L_2$ are connected in the first stage of the system. An input voltage is supplied from the PV source and the output is taken from the load resistance (R). similarly capacitors $C_1$&$C_2$ are connected in the first stage and capacitors $C_3$,$C_4$ and $C_5$ are connected in the second stage.

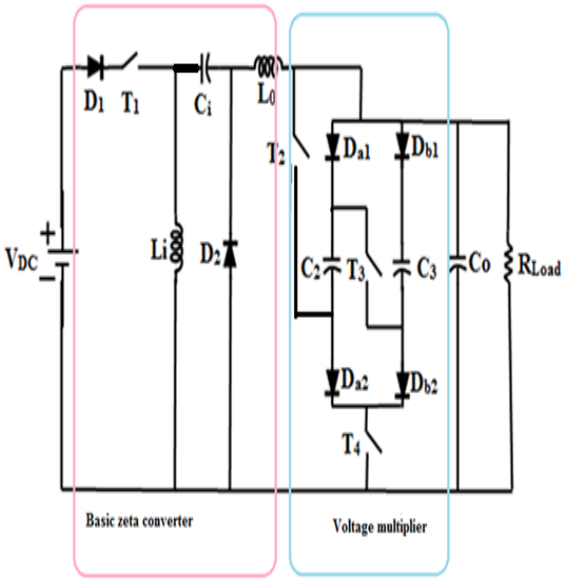


**Fig**. 2. Circuit diagram of proposed modified Zeta Converter

### *2.1 MODES OF OPERATION*

**Mode I:**

In the mode I, as shown in **Fig** 3, the switches $T_1$,$T_2$ and $T_3$ are in ON position. So the diode $D_1$ is made OFF and so the capacitor $C_1$ gets charged. The current is drawn from the source $V_{in}$ and flows through the inductors $L_i$ and $L_0$ called as charging mode. Similarly the diodes $D_3$,$D_4$, $D_5$ and $D_6$ are turned ON. During this mode, the capacitors form a series circuit and so the output voltage $V_o$ is sum of the voltages across $C_2$,$C_3$ and the input voltage $V_{in}$. Thus the output voltage at the capacitor $C_o$ is greater than the input voltage $V_{in.}$

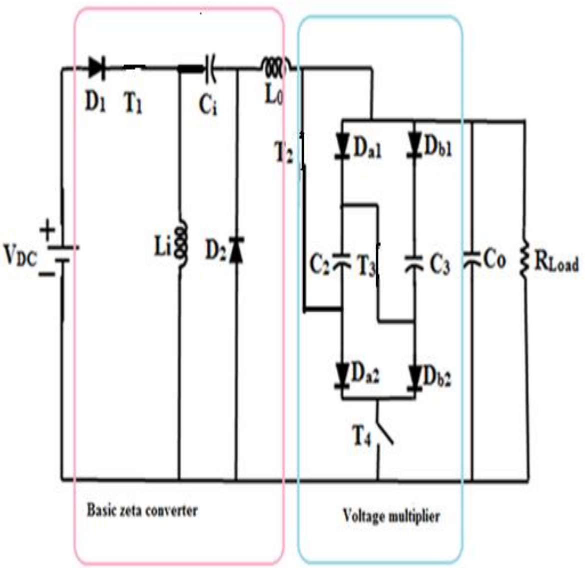


**Fig**. 3. Modes I operation of the proposed system

**Mode II:**

In mode II, the switches $T_1$ and $T_2$ & $T_3$ are changed to OFF position and the switch $T_4$ are turned in ON position as shown in the **Fig** 4. Now the diodes $D_1$,$D_2$,$D_4$ and $D_6$ are in conduction mode and thus forming the capacitors $C_2$ & $C_3$ to be connected in parallel. This connection gives the same voltage at the output capacitor $C_o$ as that of the capacitors $C_2$&$C_3$. The voltages across the capacitors $C_2$&$C_3$ are determined by the charging levels of capacitors. Now the output voltage $V_o$ is the sum of the input voltage and the voltages available in the capacitors $C_3$&$C_4$.

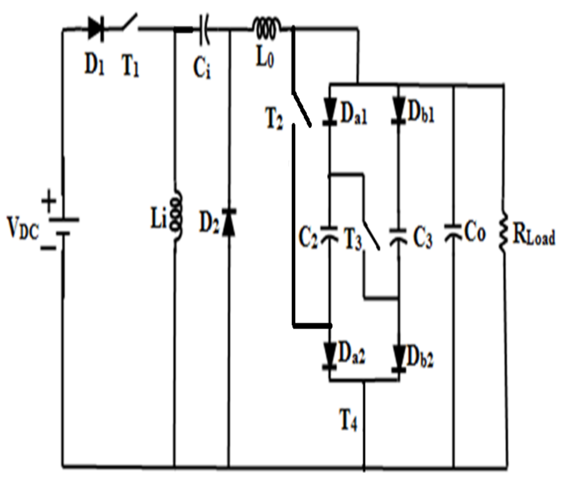


**Fig**. 4. Mode II operation of the proposed system

## 5. Converter Design

The design of circuit components such as inductors, capacitors, diodes and expression for total voltage gain [9]and losses are explained in this section. **Fig** 5 depicts the waveforms representing the steady state current of $i_{L1}$, $i_{L2}$, $i_{in}$, $i_{c1}$, $i_{c2}$, at various points in time. The average voltages across the inductor during the charging and discharging time periods will be equal to zero at steady state operation. By applying second order voltage balance equation,

$$\int_0^T VL_2 = \int_0^{DT} V_s + VC_{n+1} - V_O + \int_0^{((1-D)T} (-Vo)di \quad (1)$$

$$V_S D + V_{Cn+1} D - V_O = 0 \quad (2)$$

$$V_S = \frac{D}{(1-D)} V_{in} \quad (3)$$

The output voltage of an improved high gain converter is

$$Vo = (n+1)Vs \quad (4)$$

where n denotes the quantity of capacitors

Equations (3) and (4) define the voltage gain for the converter designed.

$$V_o = \frac{(n+1)D}{(1-D)} V_{in} \quad (5)$$

where D = $Ton/T$ is the duty ratio. (6)

### *4.1. Values of L and C parameters*

By considering the 30% percentage of ripple current, inductors $L_1$ & $L_2$ and capacitors $C_1$, $C_2$, $C_3$ and $C_4$ are calculated.
The inductor is determined using the following equation.

$$i_{L1}(t) = \frac{1}{L} \int_0^t VL1dt + I_{L11} \quad (7)$$

The ripple current in L1

$$\Delta I_{L1} = I_{L12} - I_{L11}$$

$$\Delta I_{L1} = \frac{1}{L} V_{L1} DT = \frac{V_S}{L_{1f}} \tag{8}$$

Using the Equations (4) and (8)

$$\Delta I_{L1} = \frac{(n+1)D}{L_{1f}} V_{in} \tag{9}$$

The value of inductor is

$$L_1 = \frac{(n+1)D}{\Delta IL_{1f}} V_{in} \tag{10}$$

$$\Delta I_{L2} = I_{L22} - I_{L11} = \frac{(1-D)V_0}{L_{2f}} \tag{11}$$

$$L_2 = \frac{(1-D)V_0}{f\Delta_{I2}} \tag{12}$$

It is self-evident that if the capacitors are in series, the charging currents in each capacitor are equal. To determine the values of capacitors from $C_1$ to $C_n$,

$$i_{c1} = i_{c2} = \ldots\ldots i_{cn} = -i_c = \frac{-I0}{(1-D)} \tag{13}$$

The voltage across the capacitors is determined byknowing the values of the charging currents. Therefore,

$$V_{c1} = V_{c2} = \ldots\ldots V_{cn} \tag{14}$$

$$V_{cn} = \frac{1}{cn} \int_0^{DT} i_{cn}(dt) + V_{cn}(0) \tag{15}$$

$$V_{cn} = \frac{1}{cn} \int_0^{DT} \frac{I_O}{(1-D)}(dt) + V_{cn}(0) \tag{16}$$

$$\Delta V_{c1} = \Delta V_{c2} = \ldots \Delta V_{cn} = \frac{V_O D}{(cn(1-D) f_{RL})} \tag{17}$$

The $V_{C1}$ to $V_{Cn}$ are equal, and capacitor values are determined by

$$C_1 = C_2 = \ldots C_n = \frac{V_O D}{(\Delta vcn(1-D) f_{RL})} \tag{18}$$

Then,

$$I_{in} = \frac{(n+1)DI0}{(1-D)} \tag{19}$$

If the elements are considered ideal, the proposed topology's current in the input ($I_{in}$) are given by

$$VT_i = nV_{in} \tag{20}$$

Due to the high cost of converters, the design of switches is critical. The switches are labelled $T_1$ to $T_N$ and $V_{Ti}$ is the switch voltage ratings.

$$i = 1,2,3\ldots.n$$

$$VT_1 = nV_{in} \tag{21}$$

However, the voltage rating of the switch is specified as follows

$$VT_{n+1} = \frac{(nD+1)}{(1-D)} V_{in} \tag{22}$$

Now, using Equations (20), (21), and (22), we can determine the proposed topology's total voltage as

$$VT_i + V_{T1} + V_{Tn+1} = \left( 2n + \frac{(nD+1)}{(1-D)} V_{in} \right) \tag{23}$$

### *4.2 Calculation of Losses*

The total power losses in the converter is

$$P_{cs} = V_1 I_{av} + R_s I_{rms}^{\ 2} \tag{24}$$

Switching losses must be added to the aforementioned losses. The loss is calculated as follows:

$$P_{sw.5} = f.\int_0^{t_{on}} V_S.I_S + \int_0^{t_{off}} V_S.I_S^{\ 1}(dt) \tag{25}$$

Here, $V_s$ is denoted as blocked voltage. $I_s$ and $I_s'$ denote the switching currents under different modes. The total loss is calculated by multiplying these two losses by

$$P_{sw} = P_{sw}T_1^{'} + P_{sw},T_1 + \sum_{i=1}^{n} P_{SW1}T_I \tag{26}$$

Where $P_{sw}$, $T_i'$, $T_1$, and $\Sigma\ P_{sw1}T_i$ denoted below the losses during switching.

$$\sum_{i=1}^{N} P_{sw},Ti = \frac{V_{in}V_{of}}{6RL(1-D))}(t_{on}-t_{off}) \tag{27}$$

$$P_{sw},T_1^{'} = \frac{V_{in}V_{of}Dn2}{6RL(1-D))}(t_{on}-t_{off}) \tag{28}$$

$$P_{sw},T_1^{'} = \frac{(1+nD)V_{in}V_{of}}{6RL(1-D)^2}(t_{on}-t_{off}) \tag{29}$$

Here the power loss is created due to presence of parasitic resistance of capacitor and inductor and also by some of the active and passive switches. Generally, both average and rms values of current in any inductors are same when the ripples are neglected. The parasitic loss calculation is carried out by[22] equations (30) & (31)

$$P_{L1} = \frac{v_0^2 v_{L1}}{R^2(1-d^2)} \tag{30}$$

$$P_{L2} = \frac{v_0^2(2D-D^2)^2 r_{L2}}{R^2(1-d)^4} \tag{31}$$

Hence the net loss ($P_{loss}$) is

$$P_{loss} = P_{sw} + P_c \tag{32}$$

The total loss of the proposed structure can be calculated from the Equation 30 which is the sum of conduction loss and switching loss.

## 5. Simulation and Experimental Results

The simulation diagram of the classical zeta converter is given in the **Fig** 5. The load resistance is considered as 400 Ω and the duty ratio is set as 0.8 with the input voltage as 20V.

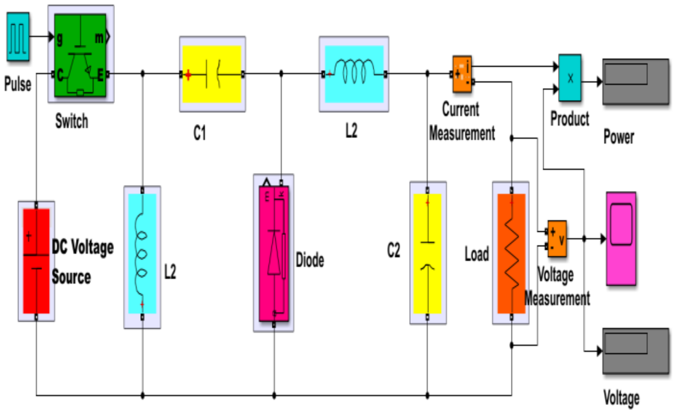


**Fig**. 5. Simulation diagram of classical zeta converter

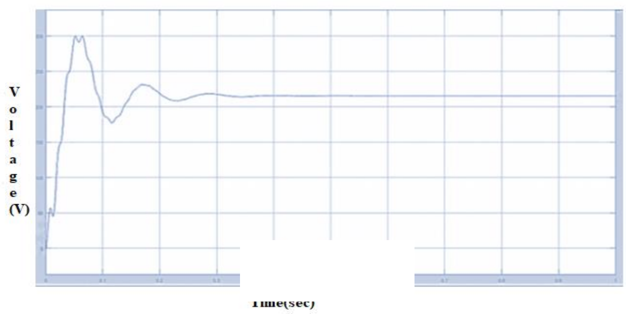


**Fig**. 6. Boosted output voltage of classical zeta converter

Fig 6 shows the simulated output voltage of the classical zeta converter where the output voltage reaches up to 190V with a duty ratio of 0.9 by considering a load resistance of 400 Ω.

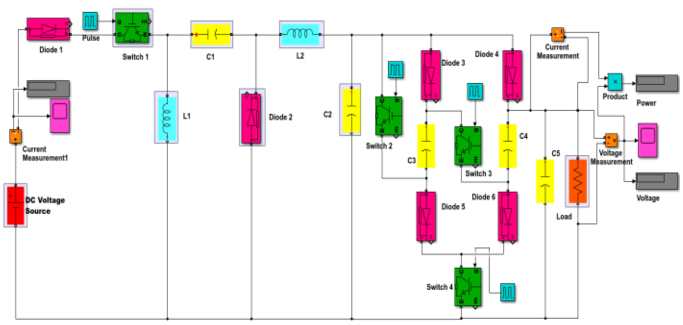


**Fig** 7. Simulation diagram of Proposed modified zeta converter

The simulation is carried out for different values of loads with a constant duty ratio by considering an input voltage of 20V.The switching frequency is fixed as 10kHz and the output voltage is taken from the load resistance.

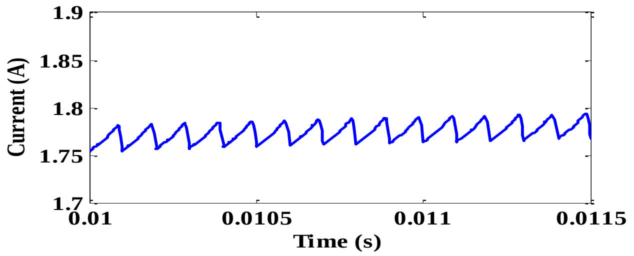


**Fig**. 8. Current through the inductor 1 of the proposed system

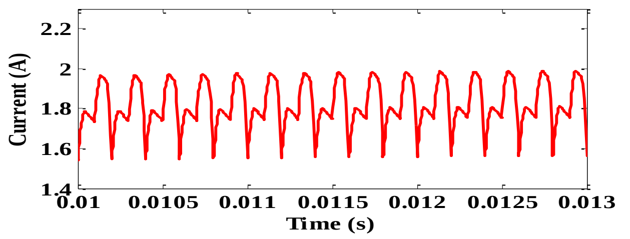


**Fig** 9. Current through inductor 2 of the proposed system

When the switch $T_1$ is closed the inductor $L_1$ charges through the diode $D_1$ and discharges through the capacitor $C_1$. The ripple through the inductor ($L_1$) is given in the Fig 7. where the current oscillates between 1.6A to 2A.

Similarly, when the switch $T_1$ is ON, the discharged current from the inductor($L_1$) will charge the inductor($L_2$) and the inductor($L_2$) current is shown in the **Fig** 9. The current through the inductor($L_2$) is oscillating from 1.75A to 1.78A.

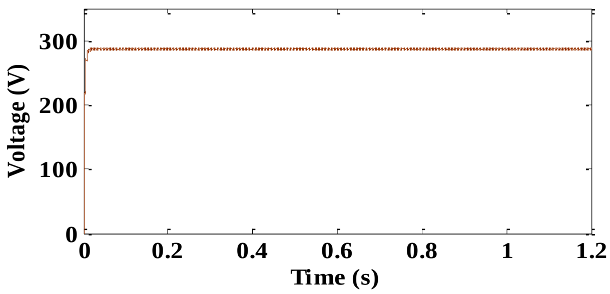


**Fig**. 10. Simulated output voltage of the proposed modified zeta converter

Fig 10 shows the simulated boosted output voltage waveform of the proposed system. The structure gives an output voltage of 290 V for a resistive load of 400Ω. Here the duty cycle is set as 0.9 and the switching frequency is set as 10kHz. The output voltage got stabilized within a short duration which is almost less than 0.1 sec.

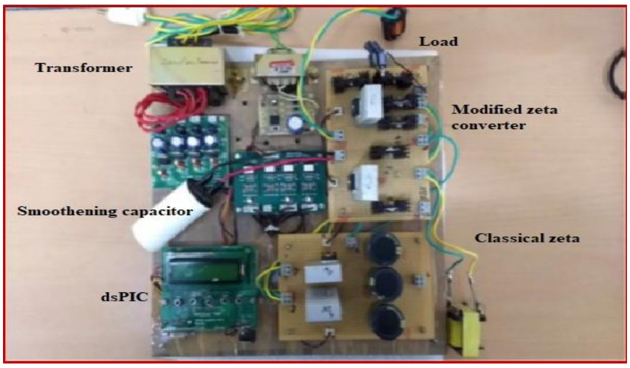


**Fig**. 11. Hardware set up of proposed modified zeta converter

The prototype model of the proposed structure is shown in the Fig 11. The structure has dsPIC controller which governs the duty cycle of the structure. A smoothening capacitor is added in the load side in order to reduce the ripples. The input voltage is given through regulated power supply and the output waveform is taken from Rigol oscilloscope.

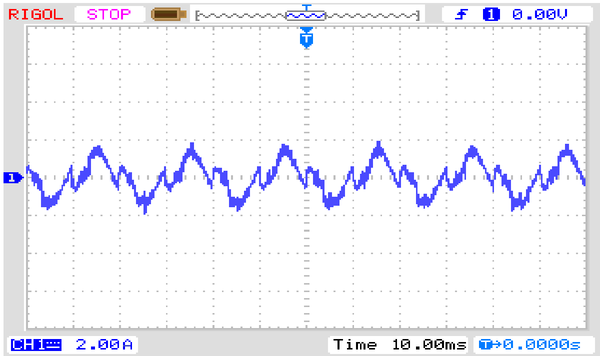


**Fig**. 12 Hardware output current through the inductor ($L_1$) of the proposed system

The Fig 12 shows the hardware current through the inductor $L_1$ where the current reaches a magnitude of 2A. The inductor current $i_{L1}$ oscillates from 1.85 A to 2.15A.

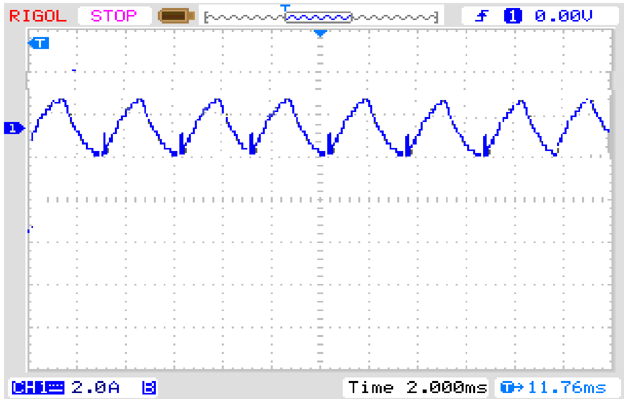


**Fig**. 13 Hardware output current through the inductor ($L_2$) of the proposed system

The Fig 13 shows the hardware current through the inductor $L_2$ where the current reaches a magnitude of 1.8A. The inductor current $i_{L2}$ oscillates from 1.65A to 1.85 A.

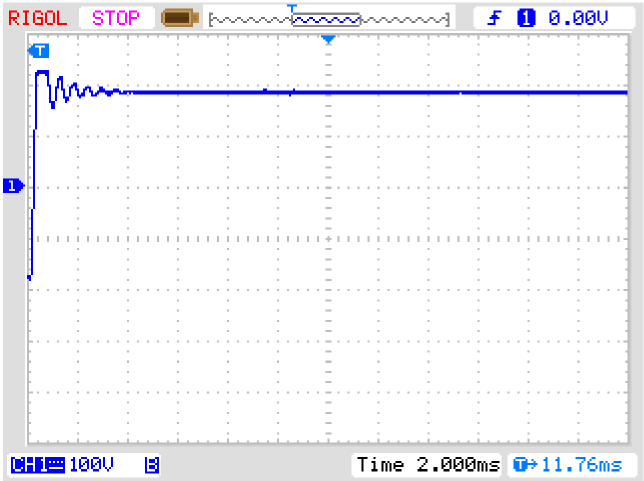


**Fig**. 14 Hardware output voltage of the proposed system

The prototype model output voltage waveform of the proposed system is shown in the **Fig** 14. Here the output voltage is reaching to 100 V for the input voltage of 20V. The output ripple is effectively reduced by the system which can be seen from the output voltage waveform. For various load conditions, the output voltage is measured which still gave a constant value. In the hardware output voltage shown in **Fig** 14, no controller has been introduced which makes the settling time to be more but can be highly reduced by properly incorporating type III controllers.

**Table 1 Hardware components of proposed topology**

| Required component | Specification | Required Number of components |
|---|---|---|
| Inductors | 0.57mH | 2 |
| Capacitors | 12.5µF, 100µF,4700µf | 4 |
| MOSFETs | IR250 | 4 |
| Diodes | BYQ28 | 5 |

The improved novel zeta converter is compared to that of other conventional converters, that are listed in Table 2. It is clear from the comparison that the developed converter topology has minimum cost and uses less number of switches. Additionally, the gain seems to be quite high in comparison to other conventional converters. Similarly table 3 and table 4 show the output voltage of the proposed system, where the voltage is maintained constant for a load resistance is changed from R=400 ohms to R=452 ohms.

**Table 2 Comparison between existing topologies and proposed topology**

| Topology | Proposed atructure | DC-DC Converter | Boost converter |
|---|---|---|---|
| Voltage | Variable | Non variable | Non variable |
| Gain of system | $\frac{(n+1)D}{(1-D)}V_{in}$ | $nV_{in}$ | $(n+1)V_{in}$ |
| Controller | Yes | No | No |
| Switches | N+1 | 2N | 3N |
| No of Capacitors | n | n+1 | n |
| Cost of system | Low | Average | Average |

**Table 3 Look up table when R=400 Ω**

| Input voltage | Duty cycle | Output voltage |
|---|---|---|
| 20 | 0.93 | 290 |
| 20 | 0.8 | 260 |
| 20 | 0.88 | 210 |
| 20 | 0.90 | 180 |
| 20 | 0.92 | 165 |

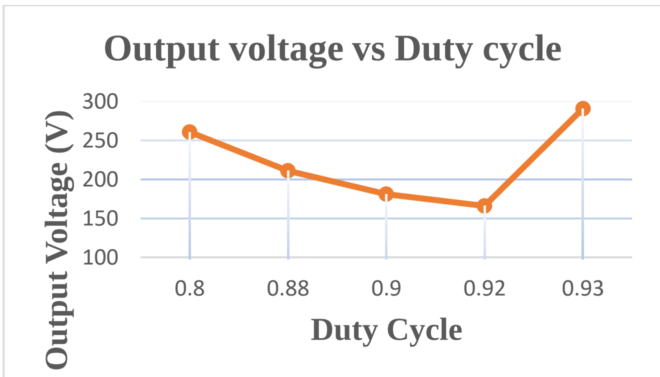


**Fig**. 15 Graph between duty cycle and output voltage

Fig 15 shows the graph between duty cycle and output voltage when the load is kept at 400 Ω with an input voltage of 20 V. Table 3 shows that the output voltage of the proposed structure gives maximum voltage when the duty ratio is fixed as 0.93. The simulation is also carried out for various duty ratio and their output voltages are found as given in the table 3.

**Table 4 when load resistance R is increased by 13%**

| Input voltage | Resistance | Output voltage |
|---|---|---|
| 20 | 400 | 290 |
| 20 | 420 | 290 |
| 20 | 440 | 290 |
| 20 | 452 | 290 |

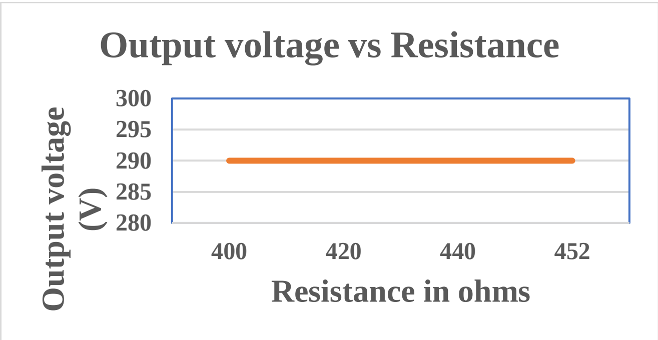


**Fig** 16 Graph between output voltage vs reistance

From the table 4, it is noticed that the output voltage remains constant even if the load resistance is increased to 13% for same input voltage. From the experimental set up of modified zeta converter, the calculated input power is 110W and the power output from the system is 104W.

Hence, the system efficiency of the proposed structure is 94% which is higher when compared to the efficiency of existing structures[22]. The reduction of 6W of power is due to losses like conduction and switching losses. The proposed structure is tested only with linear loads and in the future work nonlinear loads can be considered.

## 6. Conclusion

In this paper, a novel zeta converter is designed and simulated using MATLAB/Simulink software and the results are compared with the existing topologies. For justifying the results, a prototype model of the proposed structure is fabricated. A Mathematical model and the analysis of the proposed structure is also carried out. From the simulation results it is justified that the proposed novel zeta converter is capable of producing an output voltage of about 290 V with an input voltage of 20 V. It is seen from the results that the gain of the proposed structure is increased when compared with other similar topologies. Also, from the hardware results it is proved that the current ripples in the inductor 1 and inductor 2 are drastically reduced with minimum loss. In classical zeta converters, the output voltage cannot be made constant with change in load. But in the proposed structure, the output voltage is made constant even if the load is increased to 13% i.e., 400 Ω to 452 Ω. It is inferred from the result that the proposed system always regulates constant voltage even there is change in the load when compared to the classical zeta converter. As a result, it is possible to regulate the load voltage with variations of up to 13% in magnitude. The proposed converter offers a number of advantages, including a reduction in the number of capacitors, switches, and overall cost. The disadvantages of the voltage multiplier and classical converters are overcome by this proposed topology. Continuous input current, higher voltage gain and better regulation of output voltage are the most important features proposed topology.

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