Modified Space Vector Modulation Technique for Three Phase Three Level T-type Inverter

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Received: 16.05.2021 Accepted:26.06.2021

Abstract- Today, multi-level inverters (MLIs) are widely used and applied in many fields, including renewable energy systems and industrial drive control, among others. Multi-level inverters are mainly modulated by Pulse Width Modulation (PWM) method, in which Space Vector Pulse Width Modulation (SVPWM) is a superior method. However, as the number of levels enhances, the implementation of SVPWM for multi-level inverters has many difficulties. In this paper, the two new pulse patterns corresponding to two switching sequences in space vector modulation are applied for the three-phase three-level T-type inverter. Experimental results will evidence the advantages of the proposed switching sequences. Furthermore, both switching sequences can be executed in real-time using a single Texas Instruments F28379D, demonstrating hardware simplicity.

Keywords Multi-level inverters, Space vector pulse width modulation, T-type inverter.

1. Introduction

Multi-level inverters (MLIs) nowadays are continually being researched and developed with different modulation strategies. Some MLIs were early introduced, such as Cascaded H-bridge (CHB) [1-3], Neutral Point Clamped (NPC) [4], and Flying Capacitor (FC) [5-6]. Cascaded H-bridge inverter is suitable for photovoltaic (PV) system as it requires isolated DC sources. Though, the large number of DC sources for the higher level is the limitation of this inverter. For Neutral Point Clamped and Flying Capacitor inverter, although they only use one DC source, the number of semiconductor devices and the conduction losses are large [7]. Therefore, T-type inverter was introduced [8]. T-type inverter has many advantages of simple operating principle, a small number of semiconductor devices, low conduction losses, only one DC source needed, and good output voltage quality (low THD) [9]. Thus, T-type inverter is popular for solar rooftop systems and low voltage applications with medium switching frequency [10]. However, this topology requires the balance of two DC-link capacitors voltages. The unbalanced voltage on two DC-link capacitor causes overvoltage of semiconductor devices and high THD of the output current, so the DC-link capacitors voltage balancing algorithm is recommended. This algorithm works according to using redundant switching states during space vector modulation so there is no need for additional circuit configuration.

Sinusoidal PWM (SPWM) and space vector PWM (SVM) are commonly used to control T-type inverters, with SVM being the superior method. For the same modulation index, SVM creates the output voltage with low total harmonic distortion when compared to SPWM. The DC-link utilization of SVM is also better than SPWM. Flexibility in using switching states for minimizing switching frequency, harmonics, current ripples is also an advantage of SVM [11-22]. Nevertheless, the conventional SVM-based MLIs use complex mathematical functions to identify the location of the reference voltage vector and calculate the dwell times. For high-level inverters, the execution of SVM is a really difficult task because of a large amount of sub-triangle and redundant switching states [21]. Thus, they require complicated hardware or an expensive microcontroller. In this paper, a modified SVM technique is applied to three-phase three-level T-type inverter. The contribution of this paper is two separate switching sequences. These two switching sequences have the switching on-time directly compared with triangular wave 5 kHz, which is the same as two-level SVM. Hence, it can be easily performed on a card DSP (F28379D of Texas Instruments) [24-25]. When compared to the d-SPACE RTI 1103 platform utilized in [15], TIs DSP (TMS320F28335) and Xilinx Spartan 6 FPGA utilized in [26] this minimizes the cost and complexity of the control circuit.

2. Three Level T-type Inverter

The structure of the three-phase three-level T-type inverter is shown in Fig. 1. The input voltage is divided into two voltage components $V_{dc}/2$ by two DC capacitors. Besides, each phase consists of four IGBTs ($Sx1$ to $Sx4$, $x = A, B, C$). The switches $Sx1$ and $Sx4$ must block the entire DC-link voltage, whereas the switches $Sx2$ and $Sx3$ just must block half of it.

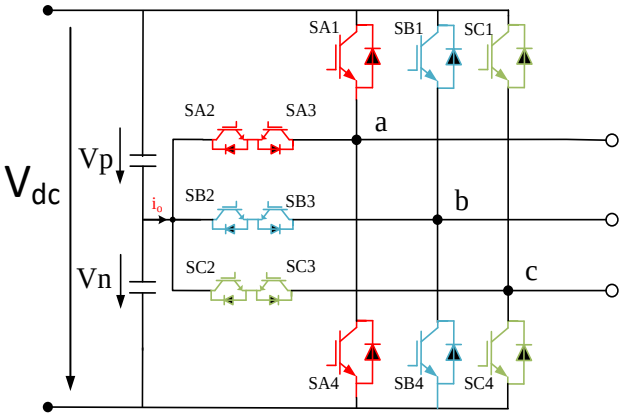


Fig. 1. Three phase three level T-type inverter.

Turning the switches ON and OFF properly, T-type inverter will generate three levels of phase voltage: $V_{dc}/2$, 0, $-V_{dc}/2$. The voltage levels $V_{dc}/2$ [P], 0 [O], $-V_{dc}/2$ [N] are obtained in the output by using different switching sequences. Table 1 describes the switching condition to get the required output voltage for phase A. A dead time must be supplied between the switching of switches to avoid DC source short circuit.

Table 1. Switching state for phase A

State	V_{out}	SA1	SA2	SA3	SA4
P	$V_{dc}/2$	ON	ON	OFF	OFF
O	0	OFF	ON	ON	OFF
N	-$V_{dc}/2$	OFF	OFF	ON	ON

3. Space Vector Modulation Technique

In three-level inverter, there are $3^3 = 27$ switching states, that can generate 19 voltage vectors, including zero vectors. These vectors are categorized into zero vector (ZV), small vector (SV), medium vector (MV), and large vector (LV). The small vectors are separated into P-type and N-type.

Table 2. Three level T-type switching states

Vector		Switching state
ZV	V0	[OOO], [PPP], [NNN]
SV	V1-V6	P-type: [POO], [PPO], [OPO], [OPP], [OOP], [POP]
		N-type: [ONN], [OON], [NON], [NOO], [NNO], [ONO]
MV	V7-V12	[PON], [OPN], [NPO], [NOP], [ONP], [PNO]
LV	V13- V18	[PNN], [PPN], [NPN], [NPP], [NNP], [PNP]

The space vector diagram is shown in Fig. 2.

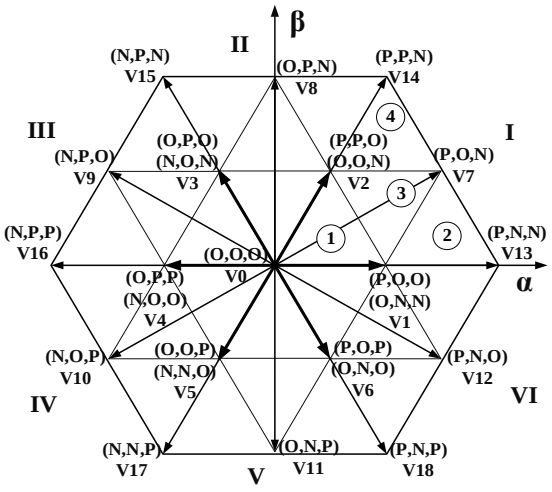


Fig. 2. Space vector diagram of three phase three level T-type inverter.

As shown in Fig. 2 space vector diagram is separated into six sectors (I to VI) and each sector has four sub-triangles (Δ1 to Δ4) with corresponding switching states.

Fig. 3 describes the SVM implementation.

3.1. abc to αβ transformation

Three phase voltage system:

$$\begin{cases} v_A = V_m \sin(\omega t) \\ v_B = V_m \sin\left(\omega t - \dfrac{2\pi}{3}\right) \\ v_C = V_m \sin\left(\omega t + \dfrac{2\pi}{3}\right) \end{cases} \quad (1)$$

Using Clarke transformation:

$$\begin{cases} v_\alpha = \frac{1}{3}\left(2v_A - v_B - v_C\right) \\ v_\beta = \frac{1}{\sqrt{3}}\left(v_B - v_C\right) \end{cases} \quad (2)$$

Output voltage vector: $V_{ref} = v_\alpha + jv_\beta$

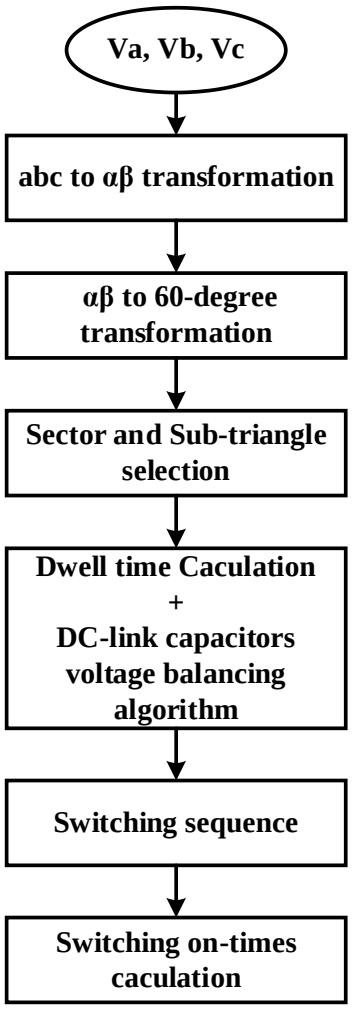


Fig. 3. The SVM implementation.

3.2. αβ to 60-degree transformation

As illustrated in Fig. 4, the vector space is made up of three coordinate systems (Z_{1x}, Z_{1y}), (Z_{2x}, Z_{2y}), and (Z_{3x}, Z_{3y}).Project $\boldsymbol{V_{ref}}$ on Z_{1x}, Z_{1y}, Z_{2x}, Z_{2y}, Z_{3x}, Z_{3y} axes:

$$V_{Z1x} = v_\alpha - tmp \qquad V_{Z1y} = 2tmp$$
$$V_{Z2x} = v_\alpha + tmp \quad V_{Z2y} = -v_\alpha + tmp \quad (3)$$
$$V_{Z3x} = 2tmp \qquad V_{Z3y} = -v_\alpha - tmp$$
$$(where\ tmp = \tfrac{1}{\sqrt{3}} v_\beta)$$

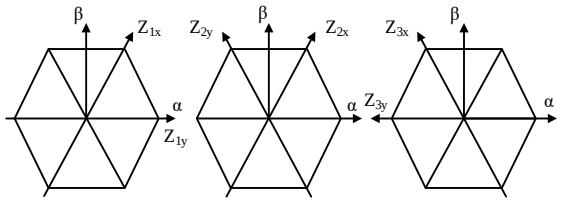


Fig. 4. 0αβ to 60-degree transformation.

3.3. Sector and sub-triangle selection

Once the V_{Zij} coordinates are found out, the location of the output voltage vector in the sectors is defined in Fig. 5.

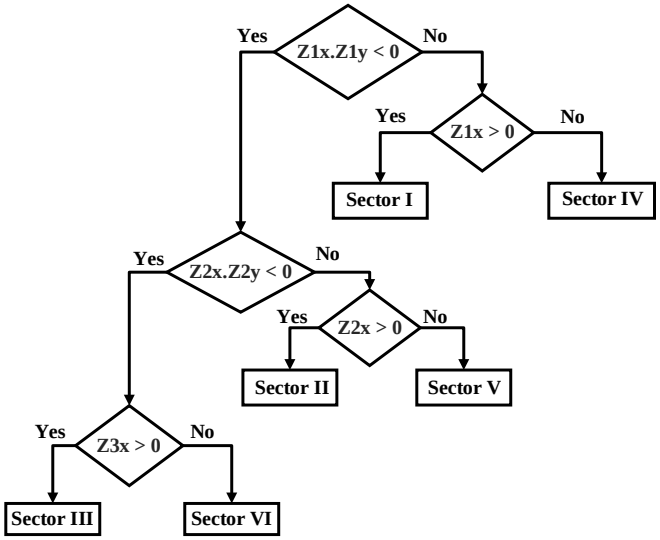


Fig. 5. Sector selection algorithm.

In three-level inverter, each sector consists of only four sub-triangles. Sub-triangle selection condition based on two quantities m_1, m_2 being the projection magnitude of $\boldsymbol{V_{ref}}$ on Z_{ij} axes.

$$\begin{cases} m_1 = \pm \dfrac{V_{Zix}}{1/3V_{dc}} \\ m_2 = \pm \dfrac{V_{Ziy}}{1/3V_{dc}} \end{cases} (i = 1-3) \quad (4)$$

The $\boldsymbol{V_{ref}}$ lies in different sub-triangle according to the following condition:

i. $\boldsymbol{V_{ref}}$ is in Δ1 if $m_1, m_2\ and\ m_1 + m_2 \le 1$

ii. $\boldsymbol{V_{ref}}$ is in Δ2 if $m_1 > 1\ and\ 2 \ge m_1 + m_2 > 1$

iii. $\boldsymbol{V_{ref}}$ is in Δ3 if $m_1 \le 1, m_2 \le 1\ and$
$2 \ge m_1 + m_2 > 1$

iv. $\boldsymbol{V_{ref}}$ is in Δ4 if $m_2 > 1\ and\ 2 \ge m_1 + m_2 > 1$

3.4. Dwell time calculation and DC-link capacitors voltage algorithm

After determining the location of the output voltage vector $\boldsymbol{V_{ref}}$ (including sector and sub-triangle), $\boldsymbol{V_{ref}}$ will be synthesized from three nearest vectors (Nearest Vector Modulation). For example, if $\boldsymbol{V_{ref}}$ lies in sub-triangle 2 of sector I, **V1**, **V7**, **V13** are three nearest vectors to $\boldsymbol{V_{ref}}$.

According to the volt-second balancing principle:

$$\begin{cases} T_S.\boldsymbol{V_{ref}} = T_a.\boldsymbol{V1} + T_b.\boldsymbol{V7} + T_c.\boldsymbol{V13} \\ T_S = T_a + T_b + T_c \end{cases}$$

$$\rightarrow \boldsymbol{V_{ref}} = \frac{T_a}{T_S}.\boldsymbol{V1} + \frac{T_b}{T_S}.\boldsymbol{V7} + \frac{T_c}{T_S}.\boldsymbol{V13} \quad (5)$$

$$\rightarrow \boldsymbol{V_{ref}} = d_a.\boldsymbol{V1} + d_b.\boldsymbol{V7} + d_c.\boldsymbol{V13}$$

Where d_a is the dwell time for **V1** and d_b, d_c is corresponding for **V7**, **V13.** Fig. 6 shows the calculation process for them.

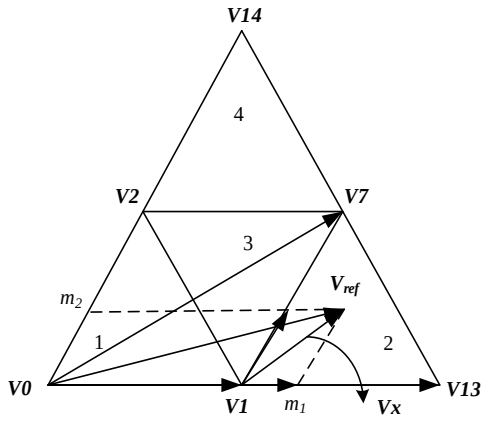


Fig. 6. Dwell time calculation for **V1, V7, V13.**

$$\begin{aligned} \boldsymbol{V_{ref}} &= \boldsymbol{V1} + \boldsymbol{Vx} \\ \rightarrow \boldsymbol{V_{ref}} &= \boldsymbol{V1} + (m_1 - 1).(\boldsymbol{V13} - \boldsymbol{V1}) + m_2.\boldsymbol{V2} \\ \rightarrow \boldsymbol{V_{ref}} &= \boldsymbol{V1} + (m_1 - 1).(\boldsymbol{V13} - \boldsymbol{V1}) + m_2.(\boldsymbol{V7} - \boldsymbol{V1}) \\ \rightarrow \boldsymbol{V_{ref}} &= (2 - m_1 - m_2).\boldsymbol{V1} + (m_1 - 1).\boldsymbol{V13} + m_2.\boldsymbol{V7} \end{aligned} \quad (6)$$

As mentioned, DC-link capacitors voltage balancing is a major challenge for T-type inverter. DC-link capacitors voltage balancing algorithm uses redundant switching states during space vector modulation. The zero vectors, the medium vectors, and the large vectors do not affect the voltage on two capacitors. Switching states of the small vectors are separated into P-type and N-type. The P-type states make i_o flow in the negative direction, C1 charge and C2 discharge, whereas the N-type states make i_o flow in the positive direction, C1 discharge and C2 charge.

DC-link capacitors voltage balancing algorithm is performed as Fig. 7:

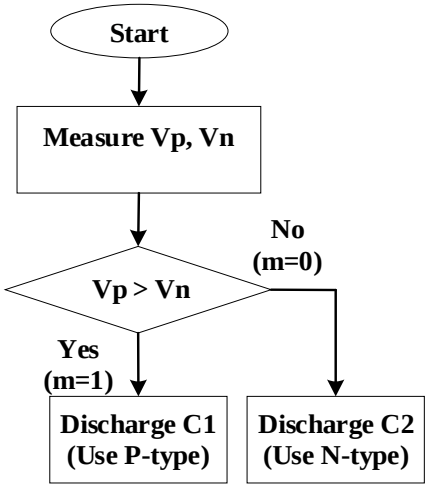


Fig. 7. DC-link capacitors voltage balancing algorithm.

The two proposed switching sequences in this paper are expounded to simplify the SVM implementation.

3.5. Switching sequence and switching on-times calculation

❖ *Eight-segment switching sequence*

The eight-segment switching sequence uses both P-type and N-type switching states of the small vectors in each case $m = 1$ or $m = 0$. Table 3 shows the eight-segment switching sequence for sub-triangle 1 ($\Delta 1$) in sector I. The purpose of this sequence is that the generated pulses have a special rule:

- Pulses feeding to switches $Sx1$ will locate on the sides.
- Pulses feeding to switches $Sx4$ will locate in the middle.

($Sx3 = \overline{Sx1}$ and $Sx2 = \overline{Sx4}$ where $x = A, B, C$).

This sequence has the advantages of low total harmonic distortion and reduced conduction losses (only one phase must change state at each switching). However, using both switching states of the small vectors in each case $m = 1$ or $m = 0$ will reduce the efficiency of DC-link capacitors voltage balancing algorithm.

Table 3. The eight-segment switching sequence for $\Delta 1$, Sector I

Δ	m	Switching state
1	$m = 1$	[PPP]→[PPO] → [POO] → [OOO] → [OOO] → [POO] → [PPO] → [PPP]
	$m = 0$	[OOO] → [OON] → [ONN] → [NNN] → [NNN] → [ONN] → [OON] → [OOO]

From Table 3, the pulse is drawn as Fig. 8.

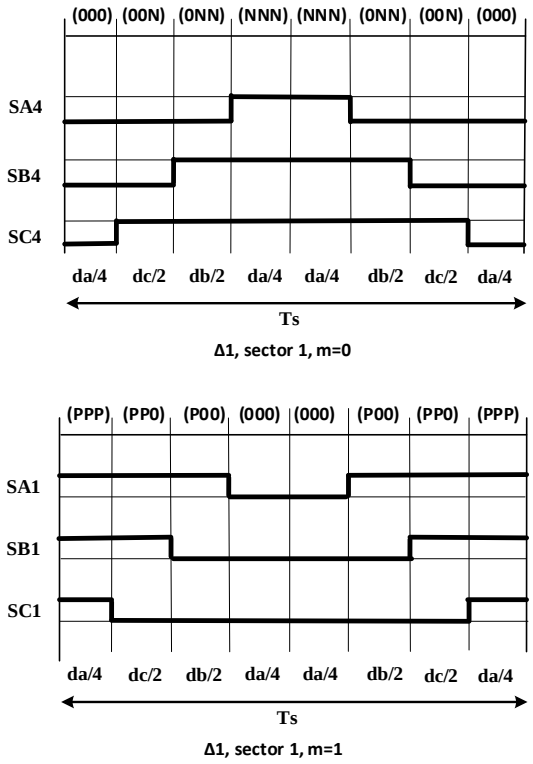


Fig. 8. The pulses for eight-segment switching sequence (V_{ref} is in Δ1, Sector 1).

To generate the pulses in Fig. 9, the switching on-times are calculated in Table 4, in which two rules are used:

- Switches $Sx1$ will apply the rule: d_{Sx1} > triangular wave.
- Switches $Sx4$ will apply the rule: triangular wave > d_{Sx4} where $x = A, B, C$).

Table 4. The switching on-times for the eight-segment switching sequence (V_{ref} is in Δ1, Sector 1)

m	Switching on-times	
$m = 1$	$d_{SA1} = \frac{d_a}{2} + d_b + d_c$	$d_{SA4} = 1$
	$d_{SB1} = \frac{d_a}{2} + d_c$	$d_{SB4} = 1$
	$d_{SC1} = \frac{d_a}{2}$	$d_{SC4} = 1$
$m = 0$	$d_{SA1} = 0$	$d_{SA4} = \frac{d_a}{2} + d_b + d_c$
	$d_{SB1} = 0$	$d_{SB4} = \frac{d_a}{2} + d_c$
	$d_{SC1} = 0$	$d_{SC4} = \frac{d_a}{2}$

❖ *Six-segment switching sequence*

The six-segment switching sequence is performed according to the following principle:

- if $m = 1$ we will select the P-type switching states.
- if $m = 0$ we will select the N-type switching states.

Table 6 shows the six-segment switching sequence for sub-triangle 1 (Δ1) in sector I. Similar to the eight-segment switching sequence, this sequence also generates the pulses having a special rule:

- Pulses feeding to switches $Sx1$ will locate on the sides.
- Pulses feeding to switches $Sx4$ will locate in the middle.

($Sx3 = \overline{Sx1}$ and $Sx2 = \overline{Sx4}$ where $x = A, B, C$).

The advantage of this sequence is that during a modulation cycle only two switches have to switch state so the conducting losses are automatically reduced to about 2/3 of the initial value [23]. In addition, using each switching state of the small vectors in two cases $m = 1$ and $m = 0$ helps to balance the DC-link capacitors voltage better, but it increases THD of the output voltage.

Table 5. The six-segment switching sequence for Δ1, Sector I

Δ	m	Switching state
1	$m = 1$	[PPO]→[POO] → [OOO] → [OOO] → [POO] → [PPO]
	$m = 0$	[OON] → [ONN] → [NNN] → [NNN] → [ONN] → [OON]

From Table 5, the pulse is drawn as follow.

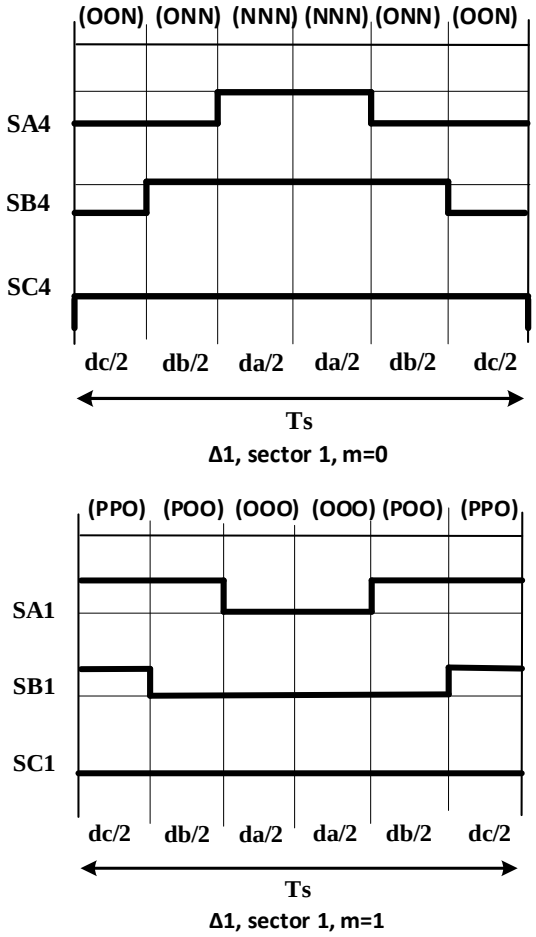


Fig. 9. The pulses for six-segment switching sequence (V_{ref} is in Δ1, Sector 1).

The switching on-times are calculated in Table 6, in which two rules are used:

- Switches $Sx1$ will apply the rule: d_{Sx1} > triangular wave.
- Switches $Sx4$ will apply the rule: triangular wave > d_{Sx4} where $x = A, B, C$).

Table 6. The switching on-times for the six-segment switching sequence (V_{ref} is in Δ1, Sector 1)

m	Switching on-times	
$m = 1$	$d_{SA1} = d_b + d_c$	$d_{SA4} = 1$
	$d_{SB1} = d_c$	$d_{SB4} = 1$
	$d_{SC1} = 0$	$d_{SC4} = 1$
$m = 0$	$d_{SA1} = 0$	$d_{SA4} = d_b + d_c$
	$d_{SB1} = 0$	$d_{SB4} = d_c$
	$d_{SC1} = 0$	$d_{SC4} = 0$

4. Experimental Results

The real-time implementation of the modified space vector modulation for three-level T-type inverter has been conducted by using card F28379D and Typhoon HIL 402. The Typhoon HIL Control Center (ver 2020.3) was used to create three-level T-type inverter with LC filter and R load. The Code Composer Studio (ver 9.3.0) was employed to implement the control algorithm. The prototype of the experiment is shown in Fig. 10.

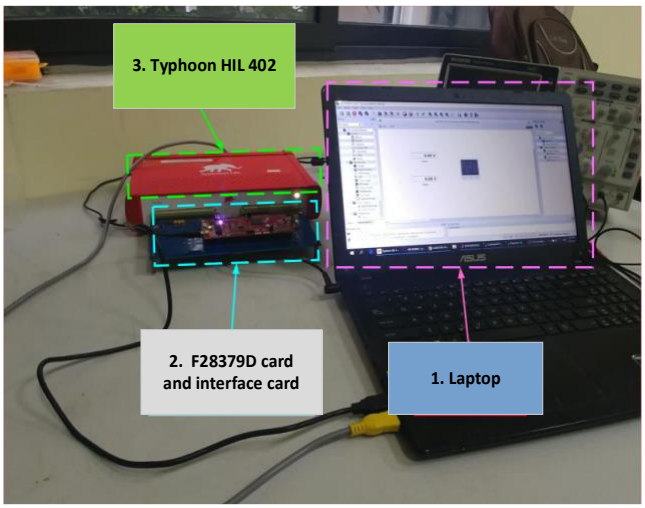


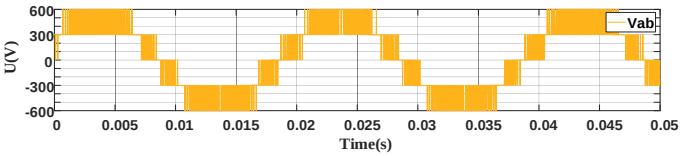
Fig. 10. The experiment environment.

The same parameters and operating conditions are applied for two proposed switching sequences to compare their performance. Particularly, the results of the output voltage, DC-link capacitor voltage, and the voltage harmonic spectrum will be presented. The parameters of the system are listed in Table 7.

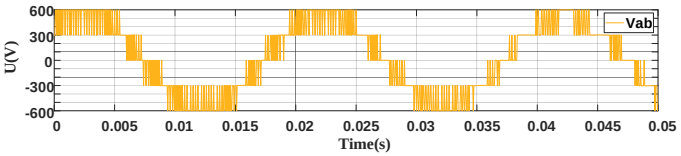
Table 7. System parameters

Parameter	Value	Description
V_{dc}	600 [V]	DC-link voltage
C	940 [µF]	DC-link capacitance
L_f	1 [mH]	Filter inductance
C_f	20 [µF]	Filter capacitance
R_{load}	9.68 [Ω]	Load resistance
f_s	5 [kHz]	Switching frequency
T_s	0.2 [ms]	Sampling time
Desired output phase voltage: 220 (V)		

Fig. 11, Fig. 12 shows the line to line u_{ab} and the output phase voltage of two switching sequences. Both line voltages u_{ab} are in five-level. It has proven that the control algorithm works properly.

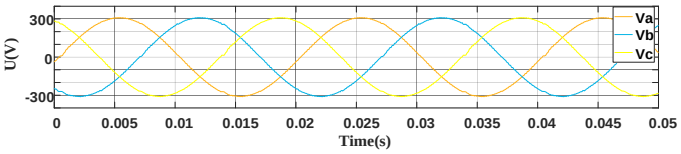


(a)

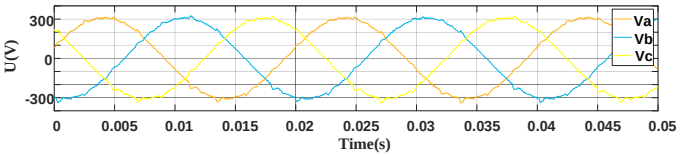


(b)

Fig. 11. The line to line u_{ab} (a) Eight-segment (b) Six-segment.



(a)



(b)

Fig. 12. The phase output voltage (a) Eight-segment (b) Six-segment.

Fig. 13 shows the DC-link capacitor voltage of two switching sequences. Using P-type and N-type switching state of the small vectors in two cases, $m = 1$ and $m = 0$ respectively, allows to balance the DC-link capacitors voltage of six-segment better than eight-segment switching sequences. As shown in Fig. 13, the $\Delta V_{pn}max$ of six-segment and eight-segment switching sequences is 7 (V) and 10 (V) respectively.

It proves that the DC-link capacitors voltage balancing algorithm works effectively.

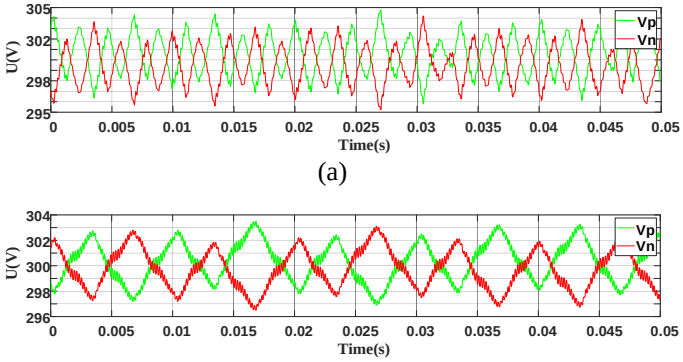


Fig. 13. The DC-link capacitor voltage (a) Eight-segment (b) Six-segment.

Fig. 14 shows the THD of the output phase voltage of two switching sequences. The quality of the output voltage of eight-segment is better, about 1.30% vs 3.11% of the six-segment switching sequence.

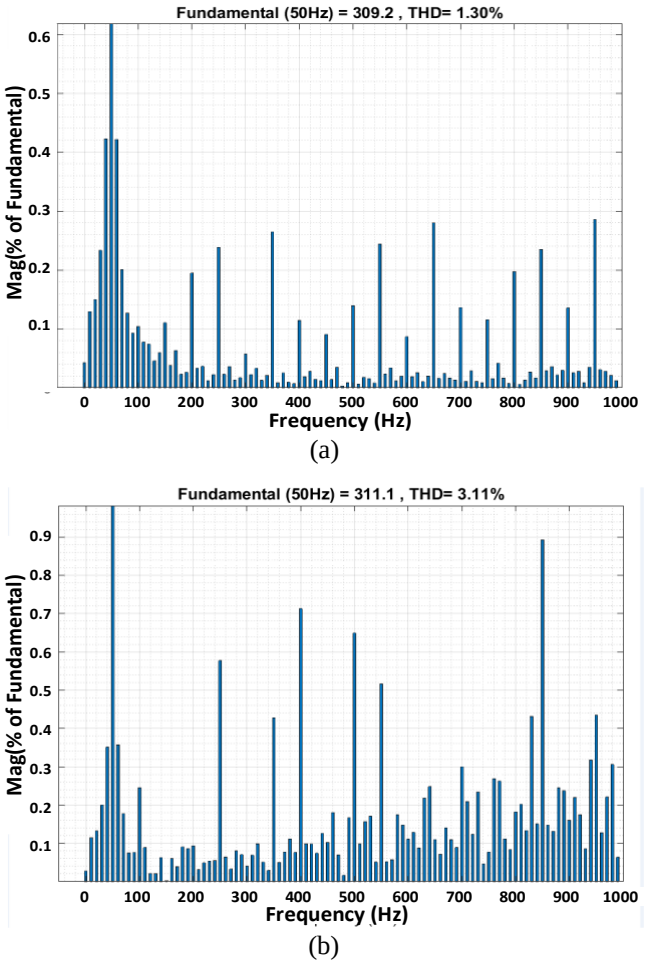


Fig. 14. The THD of the output phase voltage (a) Eight-segment (b) Six-segment.

5. Conclusions

This paper presents a modified space vector modulation technique for three-level T-type inverter. It is worth noting that two switching sequences are proposed. A comparison between two switching sequences was also presented to clarify their advantages. The way to do the switching sequences allows them to be implemented on a single Texas Instruments F28379D. This indicates a reduction in the cost and complexity of the control circuit as compared to the control circuit utilized in existing traditional methods. The real-time implementation was conducted to prove their efficiency and feasibility.

References

[1] M. Malinowski, K. Gopakumar, J. Rodriguez, and M. A. Pé. Andrez, "A Survey on Cascaded Multilevel Inverters," *IEEE Trans. Ind. Electron.*, vol. 57, pp. 2197–2206, 2010.

[2] G. Schettino, V. Castiglia, P. Livreri, R. Miceli, F. Viola, R. Rizzo, "Novel Computational Method for Harmonic Mitigation for Three-phase Five-level Cascaded H-Bridge Inverter", *2018 International Conference on Smart Grid (icSmartGrid)*, Nagasaki, Japan, pp. 299-306, 4-6 Dec. 2018.

[3] M. Keddar, M. L. Doumbia, M. D. Krachai, K. Belmokhtar, A.H Midoun, "Interconnection Performance Analysis of Single Phase Neural Network Based NPC and CHB Multilevel Inverters for Grid-Connected PV Systems", International Journal of Renewable Energy Research, Vol.9, No.3, September, 2019

[4] J. Rodriguez, S. Bernet, P. K. Steimer, I. E. Lizama "A Survey on Neutral-Point-Clamped Inverters" *IEEE Transactions on Industrial Electronics*, Year: 2010, Volume: 57, Issue: 7, Pages: 2219 2230.

[5] Jun-ichi Itoh, Ryoichi Ishibashi, Keisuke Kusaka, "Control Method of Flying Capacitor Converter Operated in Discontinuous Current Mode for High Voltage Photovoltaic Cell", *2018 International Conference on Smart Grid (icSmartGrid)*, Nagasaki, Japan, pp. 214-219, 4-6 Dec. 2018.

[6] J. Huang, K. A. Corzine, "Extended operation of flying capacitor multilevel inverters", *IEEE Trans. on Power Electronics*, Vol. 21, No. 1, pp.140-147, 2006

[7] S. Majumdar, R. Raushan, B. Mahato, K. C. Jana, P. Thakura, S. K. Singh, "Comparative Study of Space Vector Pulse Width Modulation based T-Type Three-level Inverter" *International Journal of Engineering Research & Technology (IJERT)*, Year: 2016, Volume: 4, Issue: 2, Pages: 1-5

[8] M. Schweizer, I. Lizama, T. Friedli, J. W. Kolar "Comparison of the chip area usage of 2-level and 3-level voltage source converter topologies", *IECON 2010 - 36th Annual Conference on IEEE Industrial Electronics Society*, Year: 2010, Pages: 391-396.

[9] Hyunjin Shin, Kwanghee Lee, Jaeho Choi, Seokchan Seo, Jingook Lee "Power loss comparison with different PWM methods for 3L-NPC inverter and 3L-T type inverter",

2014 International Power Electronics and Application Conference and Exposition, Year: 2014, Pages: 1322-1327.

[10] M. Schweizer, J. W. Kolar "Design and Implementation of a Highly Efficient Three Level T-Type Converter for Low-Voltage Applications", *IEEE Transactions on Power Electronics*, Year: 2013, Volume: 28, Issue: 2, Pages: 899-907.

[11] C. Bharatiraja, J. L. Munda, Ramazan Bayindir, Mohd Tariq, "A common-mode leakage current mitigation for PV-grid connected three-phase three-level transformerless T-type-NPC-MLI", *2016 IEEE International Conference on Renewable Energy Research and Applications (ICRERA)*, Birmingham UK, pp. 578-583, 20-23 Nov. 2016.

[12] V. Fernão Pires, D. Foito, T. G. Amaral, "Fault Detection and Diagnosis in a PV Grid-Connected T-Type Three Level Inverter", *2015 International Conference on Renewable Energy Research and Applications (ICRERA)*, Palermo Italy, pp. 933-937, 22-25 Nov. 2015.

[13] Habib Benbouhenni, "Comparative Study Between Direct Vector Control and Fuzzy Sliding Mode Controller in Three-Level Space Vector Modulation Inverter of Reactive and Active Power Command of DFIG-Based Wind Turbine Systems", International Journal of Renewable Energy Research, Vol.2, No.4, December 2018.

[14] A. Bellini, S. Bifaretti, "Comparison between Sinusoidal PWM and Space Vector Modulation Techniques for NPC Inverters" *IEEE Russia Power Tech*, Year: 2005, Pages: 1-7.

[15] K. C. Jana, S. K. Chowdhury, and S. K. Biswas, "Performance evaluation of a simple and general space vector pulse-width modulation-based M-level inverter including over-modulation operation", *IET Power Electron.*, vol. 6, no. 4, pp. 809–817, 2013.

[16] K. C. Jana and S. K. Biswas, "Generalised switching scheme for a space vector pulse-width modulation-based N-level inverter with reduced switching frequency and harmonics", *IET Power Electron*., pp. 1–9, 2015.

[17] K. Gupta and A. M. Khambadkone, "A general space vector PWM algorithm for multilevel inverters, including operation in overmodulation range", *IEEE Trans. Power Electron.*, vol. 22, no. 2, pp. 517–526, 2007.

[18] Y. Deng, K. H. Teo, C. Duan, T. G. Habetler, R. G. Harley, 'A fast and generalized space vector modulation scheme for multilevel inverters', *IEEE Trans. Power Electron.*, 2014, 29, (10), pp. 5204–5217.

[19] S. Vasudevamurthy and Swetha, "Simulation And Comparison Of Space Vector Pulse Width Modulation For Three Phase Voltage Source Inverter," *Int. J. Eng. Res. Technol.*, vol. 2, no. 5, pp. 1691–1698, 2013.

[20] Duc-Tri Do, Minh-Khai Nguyen, Thanh-Hai Quach, Vinh-Thanh Tran, Cong-Bang Le, Kyoung-Won Lee, andGeum-Bae Cho, "Space Vector Modulation Strategy for Three-Level Quasi-Switched Boost T-Type Inverter", *2018 IEEE 4th Southern Power Electronics Conference (SPEC)*, Singapore, 10-13 Dec. 2018.

[21] Sajitha M. and Ramchand R., "Space Vector PWM Scheme for Three Phase Three Level T-type NPC Inverter", *2019 2nd International Conference on Intelligent Computing, Instrumentation and Control Technologies (ICICICT)*, Kannur India, pp. 523-528, 5-6 July 2019.

[22] C. Qin, C. Zhang, A. Chen, X. Xing, G. Zhang, "A Space Vector Modulation Scheme of Quasi-Z-Source Three-Level T-Type Inverter for Common-Mode Voltage Reduction", *IEEE Trans. Ind. Electron.*, vol. 65, no. 10, pp. 8340-8350, Oct. 2018.

[23] Nguyen Phung Quang, Jörg-Andreas Dittrich, *Vector Control of Three-Phase AC Machines – System Development in the Practice*, 1st ed., Springer, 2008, pp. 49-51.

[24] D. Kairous, R. Wamkeue, J.J. Beaudoin, "DSP-Based SVM Generation Algorithm For DFIM", *2013 IEEE Electric Power Conference (EPEC)*, Halifax NS Canada, 21-23 Aug. 2013.

[25] B. J. Pordanjani, A. Saleki, M. T. Bina, "DSP-Implementation of the SVM and THI-PWM Techniques: Comparing THD and Switching Losses of Cascaded H-Bridge Converter", *28th Iranian Conference on Electrical Engineering (ICEE)*, Tabriz Iran, 4-6 Aug. 2020.

[26] X. Li, S. Dusmez, B. Akin, K. Rajashekara, "A New SVPWM for Phase Currents Reconstruction of Three-Phase Three-Level T-type Converters", *2015 IEEE Applied Power Electronics Conference and Exposition (APEC)*, Charlotte NC USA, pp. 1582-1588, 15-19 March 2015.