Comparison of Non-isolated High Gain Multi-input DC-DC Converters

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Abstract- In this paper, couple of non-isolated high gain multi-input DC-DC converter (MIC) topologies are presented and their salient features are compared. Each of the high gain MICs are synthesized from two identical high gain (HG) DC-DC converter structures. The input power supply to each of the MIC topologies comprising of two parallel connected HG converters is obtained from two separate sources. The individual outputs of the two HG converters are connected in parallel with each other through ORing diodes and deliver the required load power. The individual HG converter is developed from an interleaved boost converter (IBC) configuration. Its voltage gain is enhanced by judiciously adopting hybrid combination of various gain extension techniques like (i) coupled inductors (CI), (ii) voltage-lift (VL) technique, (iii) diode capacitor multiplier cells (DCM) and (iv) voltage multiplier cells (VMC). The presented MIC topologies yield a voltage gain of about 10.33 and 21.11 at 200W power level. Moreover, experimental results demonstrate the power sharing concept of both the MICs when both the input sources are available. In addition, the ruggedness of the proposed MIC structure is clearly validated through the experimental results obtained when only one source supplies the load.

Keywords Multi-input High Gain DC-DC Converter; Voltage multiplier cells; Interleaving; ORing diodes; Current sharing.

1. Introduction

Renewable energy sources (RES) such as solar, wind, biomass etc are having a deep positive impact in the manner in which electrical energy is being consumed. With particular reference to India, the country's increased focus on developing alternative sources of energy is well-understood by the total energy consumption and the target set for the year 2030 [1]. Advances in renewable energy-based systems are posing interesting challenges to power electronic converters which are located between the source and load. These converters play a major role in voltage transmission ratio and efficiency. Furthermore, with advancements in renewable energy technologies, hybrid energy sources are gaining importance and need to be integrated in a coordinated manner [2, 3]. Multi-input converters play a very important role in integrating various renewable energy sources with the common bus [4].

To achieve high voltage gain values, generally gain extension techniques are adopted. Voltage multiplier cells (VMC), voltage lift (VL), diode capacitor multiplier (DCM), switched capacitors (SC), switched inductors (SI) and combinations of these are some of them. The converters presented in [5-7] employ switched inductor and switched capacitor cells to achieve high voltage gain. However, as the voltage gain cells are introduced closer to the input and before the switches, they are subjected to high voltage stress. The voltage gain value of the converter presented in [8] is limited due to the employment of VMCs as the component

count and losses associated with the additional components increase when higher gain values of more than 10 are required. In the converters described in [9-11], high voltage gain value is obtained by adjusting the turns ratio of the CIs. Nevertheless, the input ripple content is on the higher side. By judiciously employing CIs, ripple free input current is achieved in the converter described in [12]. In [13-15], DCM is used as gain extension mechanism while the converters described in [16, 17] employ voltage-lift technique.

The non-isolated converters are classified into Single-Input Single Output (SISO), Single-Input Multi-Output (SIMO), Multi-Input Single-Output (MISO) and Multi-Input Multi-Output (MIMO) based on input and output configurations. SISO converters presented in [18, 19] use CIs to achieve high gain. They are supplied from single source to meet the required load demand. SIMO converters are developed in [20-22]. They are powered from one input and have various outputs. However, SIMO converters suffer from high voltage stress on the switches and increased component count. MISO converters have two or more number of input sources to meet a particular load demand [23, 24]. By employing suitable voltage and current control techniques, the circulating current between converters is minimised [25, 26]. In the MIMO converter presented in [27], numerous inputs and loads are connected and disconnected at any time. Nevertheless, appropriate control techniques are necessary for independent load control. Further, the presented MIMO are not capable of meeting the load requirement when one input fails. In [28], a high gain MIC which supplies the load even when only one converter operates is presented.

In this paper, two high gain multi-input converter topologies (MIC-1 and MIC-2) are proposed. Section 1 presents an overview of various MICs, their advantages and existing research gap. In section 2, the circuit diagrams of the proposed multi-input converters are described. Steady state analysis and design details of both the MICs are elaborated in Section 3. The proposed topologies are simulated and hardware results are discussed in Sections 4 and 5 respectively. Some of the main attributes of MIC-1 and MIC-2 are compared in Section 6 and the concluding remarks are encapsulated in Section 7.

2. Proposed Converters

2.1. High Gain Multi-Input Converter 1(MIC-1)

Fig. 1 shows the power circuit of proposed topology 1. The proposed topology 1 is constructed by connecting two identical converters in parallel. In this topology, two VMC's are used along with conventional boost converter in each individual converter to obtain a voltage gain of 10.33 and switches are operated at a duty ratio of 0.716. The output of converter 1 is obtained across C_{01} and converter 2 across C_{02} respectively. Both the converters are connected in parallel using ORing dodes D_{p1} and D_{p2}. The detailed analysis is given in [28].

2.2. High Gain Multi-Input Converter 2(MIC-2)

Fig. 2 shows the power circuit topology 2. In this topology also, two identical converters are connected in parallel to form high gain MIC. In this topology IBC with VL, one VMC and two DCM's are used to achieve high gain in each individual converter.

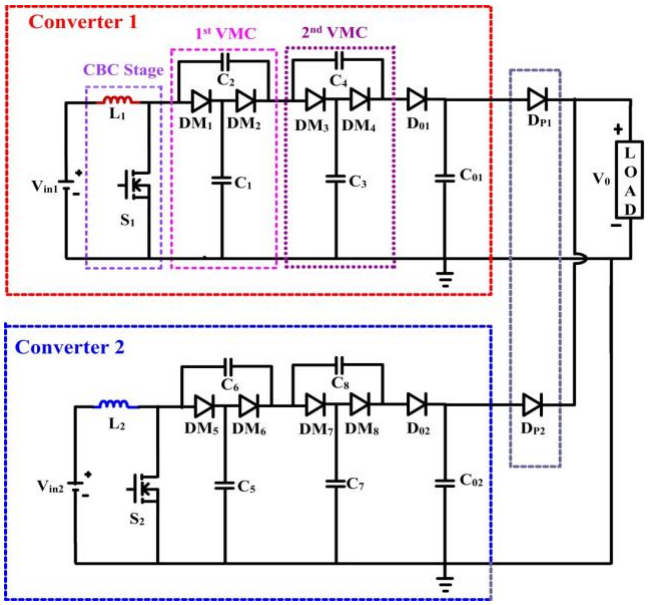

Fig. 1 Power circuit of proposed topology 1.

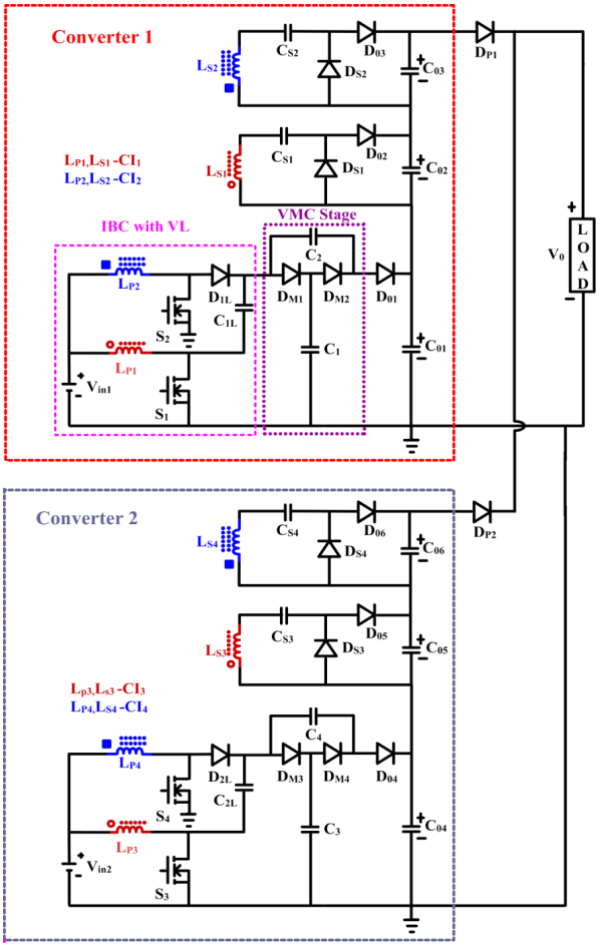

Fig. 2 Power circuit of proposed topology 2.

Switches are operated at safe duty ratio of D=0.5 and voltage gain of 21.11 is achieved. The primary windings of coupled inductors are placed in IBC and the output from IBC is lifted through Voltage Lift Cell. This voltage is uplifted with gain extension cell VMC and this voltage is collected across C_{01}. The secondary windings of CI's are connected to two DCM's and the output voltages are obtained across C_{02} and C_{03} respectively. C_{01}, C_{02} and C_{03} are cascaded to obtain the required output voltage of converter 1 of topology 2. Similar to topology 1, D_{p1} and D_{p2} serves the purpose of parallel operation.

3. Steady State Analysis

3.1. Voltage gain

In the proposed topology 1, the voltage gain of individual converter is obtained from basic principles and expressed as

$$M = M_{CBC} + M_{VMC} = \frac{1+N}{1-D} \quad (1)$$

where M is the voltage gain of topology 1, D is the duty ratio of switches and N is the number of VMCs (N=2 for the converter in topology 1).

In topology 2, the voltage gain of converter is given by

$$M = M_{IBC} + M_{VL} + M_{VMC} + M_{DCM} = \frac{2+N+2nk}{1-D} \quad (2)$$

where M is gain of topology 2, D is duty ratio, n is turns ratio, k is coupling coefficient and N = number of VMCs =1. The voltage gain value of topology 2 is twice that of topology 1. Table 1 shows the expressions for voltage gain obtained at different stages.

3.2. Voltage and current stress on the power switches

The voltage and current stress of the switches are 33.33% of output voltage and 100% of input current respectively in topology 1.

Table 1. Voltage Gain Formulae

	Voltage Gain	
	Topology 1	Topology 2
Voltage across C_{01}	$V_{C_{01}} = \frac{3}{1-D}V_{in1}$	$V_{C_{01}} = \frac{3}{1-D}V_{in1}$
Voltage across C_{02}, C_{03}	-	$V_{C_{02}} = V_{C_{03}} = \frac{n}{1-D}V_{in1}$
Voltage Gain	$\frac{1+N}{1-D}$	$\frac{2+N+2nk}{1-D}$

In topology 2, the voltage stress on the switches is only 9.47% of output voltage. The current stress is 50% of input current. Because of the interleaving technique in topology 2, the voltage and current stress are very low. Table 2 provides the expressions for computing the stress values.

3.3. Voltage stress on diodes

The voltage stress across diodes is 33.33% of output voltage in topology 1. In topology 2, the voltage stress across diodes varies from 9.47% to 35.8% of output voltage.

3.4. Design of passive components

The values of inductors and capacitors are obtained from basic principles by considering the current and voltage ripple respectively along with switching frequency. The values are presented in Table 3.

Table 2. Voltage and current stresses on semiconductor devices

	Stress on the switches		Stress on the diodes
	Voltage stress	Current stress	Voltage Stress
Topology 1	$V_{S_1} = V_{S_2} = \frac{1}{1-D}V_{in1} = 128V$ (33.33% of V_0)	$I_{S_1} = I_{S_2} = I_{in} = 2.78A$ (100% of I_{in})	$V_{DM} = \frac{V_{in}}{1-D} = 128V$ (33.33% of V_0)
Topology 2	$V_{S_1} = V_{S_2} = \frac{1}{1-D}V_{in1} = 36V$ (9.47% of V_0)	$I_{S_1} = I_{S_2} = \frac{I_{in1}}{2} = 5.55A$ (50% of I_{in})	$V_{D_{M1}} = V_{D_{M2}} = V_{D_{01}} = \frac{1}{1-D}V_{in1} = 36V$ (9.47% of V_0) $V_{D_{1L}} = \frac{2}{1-D}V_{in1} = 72V$ (18.94% of V_0) $V_{D_{S1}} = V_{D_{S2}} = V_{D_{02}} = V_{D_{03}} = \frac{nk}{1-D}V_{in1} = 135.98V$ (35.8% of V_0)

Table 3. Passive component design

	Design values of	
	Inductors	Capacitors
Topology 1	$L_1 = \frac{V_{in1}D_1}{f\Delta i_{L_1}}$ $= 375\mu H$	$C_{01} = \frac{I_0 D_1}{f\Delta v_0}$ $= 10\mu F, 450V$
Topology 2	$L_{p1} = \frac{V_{in1}D_1}{f\Delta i_{L_{p1}}}$ $= 40\mu H$ $L_{p2} = \frac{V_{in2}D_2}{f\Delta i_{L_{p2}}}$ $= 40\mu H$ $L_{s1} = n^2 L_{p1}$ $= 650\mu H$ $L_{s2} = n^2 L_{p2}$ $= 650\mu H$	$C_{01} = \frac{I_0 D_1}{f\Delta v_{C01}}$ $= 47\mu F, 250V$ $C_{02} = \frac{I_0 D_2}{f\Delta v_{C02}}$ $= 47\mu F, 250V$ $C_{03} = \frac{I_0 D_1}{f\Delta v_{C03}}$ $= 47\mu F, 250V$

where f is switching frequency, Δi_L represents inductor ripple current, I_0 represents output current and ΔV_0 represents output voltage ripple.

4. Simulation Results

The high gain multi-input converters are simulated in PSpice environment. Figs. 3 to 8 shows the simulation results of topology 1 while Figs. 9 to 14 correspond to topology 2.

4.1. Topology 1

Topology 1 is designed and simulated for 36*V*/380*V* at 200*W* power output. When an input of 36*V* is applied from both the sources, 374*V* output is achieved which translates to a voltage gain value of 10.38.

Fig. 3 shows the input voltages and input currents of the individual converters (converter 1 and 2) employed in topology 1. When both the sources are available, both the converters share the load and draw equal currents. In Fig. 4, V_{g1} and V_{g2} are gate pulses applied to switches S_1 and S_2 at a duty of 0.716. The charging and discharging profiles of inductors are clearly shown in I_{L1} and I_{L2} waveforms.

Fig. 5 shows the gain attained in each stage of converter. When 36*V* input is applied, the voltage is boosted to 126*V* in first stage and reached 251*V* at the end of second VMC stage and finally an output of 374*V* is obtained at the load. Fig. 6 shows output voltage, output currents of both the converters and total output current. When the converter is powered from equal voltage sources, the load is equally shared by both the converters. For an output of 374*V*, 519*mA* current is drawn by the load with a power output of 194*W*.

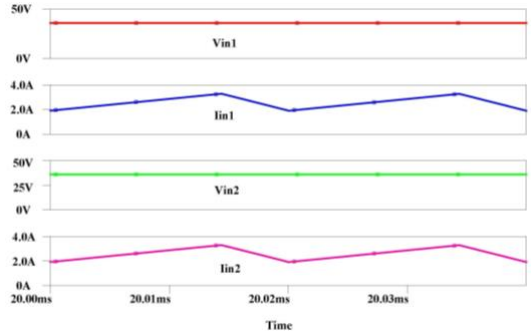

Fig. 3 Input voltage (V_{in1}), Input current (I_{in1}), Input voltage (V_{in2}), Input current (I_{in2})

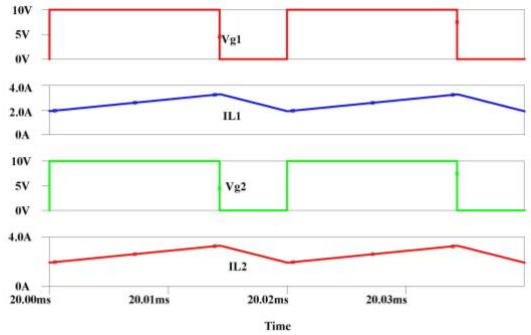

Fig. 4 Gate pulse (V_{g1}) to switch S_1, Inductor current (I_{L1}), Gate pulse (V_{g2}) to switch S_2, Inductor Current (I_{L2})

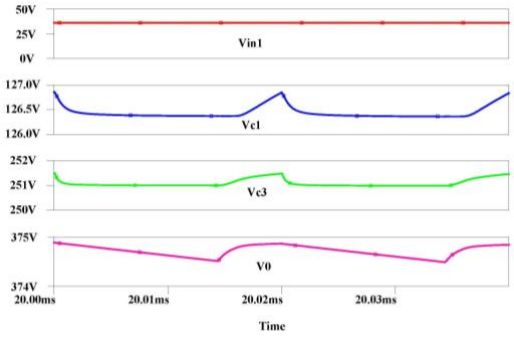

Fig. 5 Input voltage (V_{in1}), voltage across 1st VMC (V_{c1}), voltage across 2nd VMC (V_{c3}), output voltage (V_0)

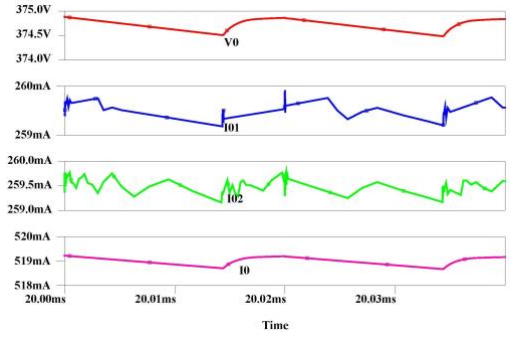

Fig. 6 Output voltage (V_0), Output current of converter 1 (I_{01}), output current of converter 2 (I_{02}), output current (I_0)

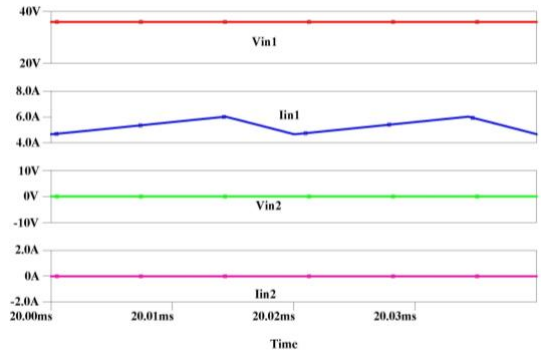

Fig. 7 Input voltage (V_{in1}), input current (I_{in1}), input voltage (V_{in2}), input current (I_{in2})

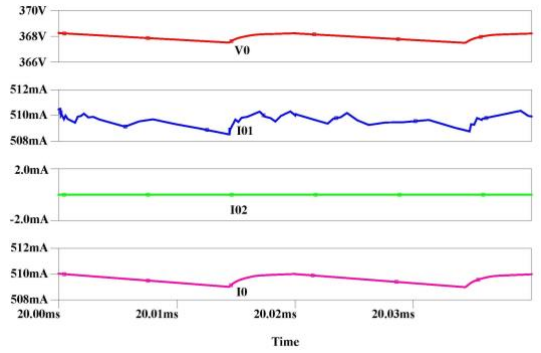

Fig. 8 Output voltage (V_0), output current of converter 1 (I_{01}), output current of Converter 2 (I_{02}), output current (I_0)

Fig. 7 and 8 shows the corresponding waveforms when any one of the sources is not available. In Fig. 7, input source of converter 2 is not available. Converter 1 alone operates by drawing the total input current of 5.6A and delivers the required power to the load while converter 2 does not contribute to the load current as its source voltage is absent. Fig. 8 validates the fact that the total load requirement is met by converter 1 alone. Since renewable energy sources are unpredictable in nature, the proposed high gain multi-input converter is designed to meet the load even when only one source is available.

4.2. Topology 2

Topology 2 is designed and simulated to operate from 18V inputs, provide 380V to the load at 200W output power. The switches employed in topology 2 are operated at a duty ratio of D=0.5 and the CIs are designed with turns ratio of n=4. When an input of 18V is applied from both the sources, 372V output is achieved which translates to a voltage gain value of 20.67.

Fig. 9 shows the input voltages and input currents of converter 1 and 2 in topology 2. When 18V is applied, each converter draws 11A.

Fig. 10 shows the gate pulses applied to switches S_1 and S_2 and current flowing through the primary windings of CI's. Since an IBC is used, the gate pulses are complementary to each other.

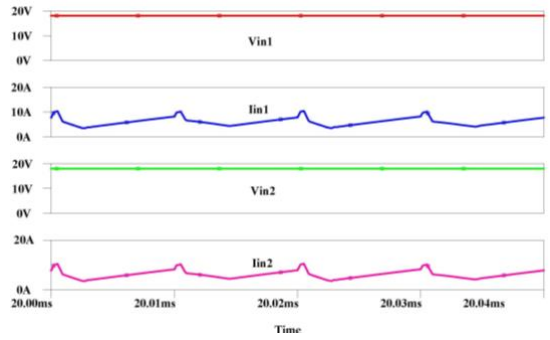

Fig. 9 Input voltage (V_{in1}), input current (I_{in1}), input voltage (V_{in2}), input current (I_{in2})

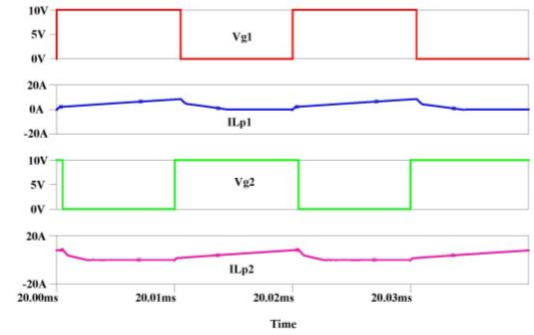

Fig. 10 Gate pulse (V_{g1}), inductor current (I_{Lp1}), Gate pulse (V_{g2}), inductor current (I_{Lp2})

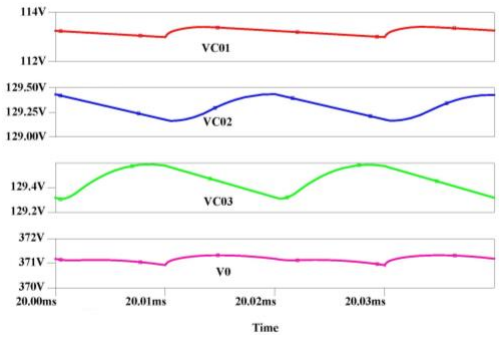

Fig. 11 Voltage across C_{01} (V_{c01}), voltage across C_{02} (V_{c02}), voltage across C_{03} (V_{c03}), output voltage (V_0)

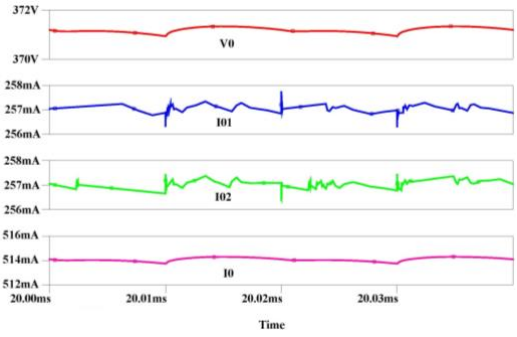

Fig. 12 Output voltage (V_0), output current of converter 1 (I_{01}), output current of Converter 2 (I_{02}), output current (I_0)

Fig. 11 shows output voltages across C_{01}, C_{02}, C_{03} and load. The voltage across C_{01} is 113V, across C_{02} and C_{03} is 129V each cascaded to 372V at the output. Fig. 12 shows output voltage, output currents of both the converters and total output current of topology 2. When V_{in1}=V_{in2}=18V, V_0=372V, I_{01}=I_{02}=257mA and I_0=514mA.

Fig. 13 and 14 shows the topology's capability to deliver the required load power even when only one of the converters (Converter 1) input is available. These figures clearly indicate the capability of converter. Since V_{in2}=0, Converter 1 alone supplies the total load and delivers 191W power to the load.

5. Hardware Results

A laboratory prototype of high gain MIC's is designed and tested. The gate pulses are generated using PIC18F45K20 microcontroller with D=0.716 for topology 1 and D=0.5 for topology 2 at a switching frequency of 50 kHz and fed to switches through IR25600 MOSFET driver.

5.1. *Topology 1*

Fig. 15 shows the gate pulses applied to switches with 0.716 duty ratio and voltage across the switches. When switch S_1 is ON, energy is stored in input inductor. When the switch S_1 is OFF, the stored energy in inductor is transferred to capacitors C_1, C_3 and C_0. When the switch is OFF, the voltage stress across switch is about 128V.

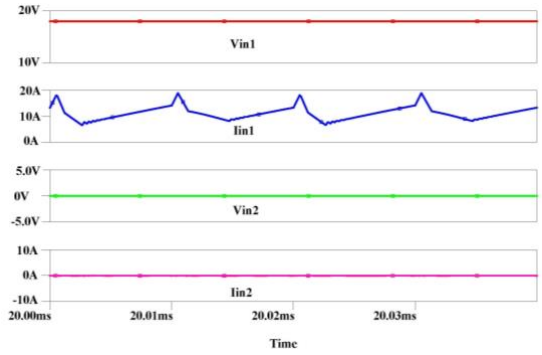

Fig. 13 Input voltage (V_{in1}), input current (I_{in1}), input voltage (V_{in2}), input current (I_{in2})

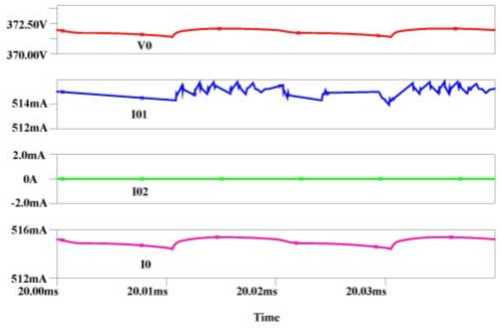

Fig. 14 Output voltage (V_0), output current of Converter 1 (I_{01}), output current of Converter 2 (I_{02}), output current(I_0)

When an input of 36V is applied from both the sources, each converter in MIC draws an input current of 2.7A. The output voltage is 372V and the output current magnitude is 520mA. Thus, a voltage gain of 10.33 is practically obtained at an output power level of 193.4W. The corresponding waveforms are depicted in Figs. 16 and 17 respectively.

The progressive voltage rise from input voltage of 36V to an output of 380V is shown in Fig. 18. When switch S_1 is OFF, the stored energy in L_1 is transferred to C_1 through DM_1, C_2 transfers to C_3 through DM_3 and C_4 transfers to C_{o1} through D_{o1}. When V_{in1} is equal to 36V, the first VMC output is 138V, the second VMC output is 240V leading to a final output voltage of about 380V.

Fig. 19 and 20 shows the voltage across multiplier diodes. When switches S_1, S_2 are ON, DM_1, DM_5, DM_3, DM_7 are reverse biased and DM_2, DM_6, DM_4, DM_8 are forward biased. During this period C_1, C_3, C_5, C_7 discharge stored energy into C_2, C_4, C_6, C_8 respectively. Figs. 19 and 20 validate the complementary operation of the diodes (DM_1 – DM_8) located in the VMC network.

5.2. *Topology 2*

Gate pulses of 0.5 duty ratio are given to interleaved boost converter switches as shown in Fig. 21. Since it is an IBC, gate pulses are phase-shifted by 180º.

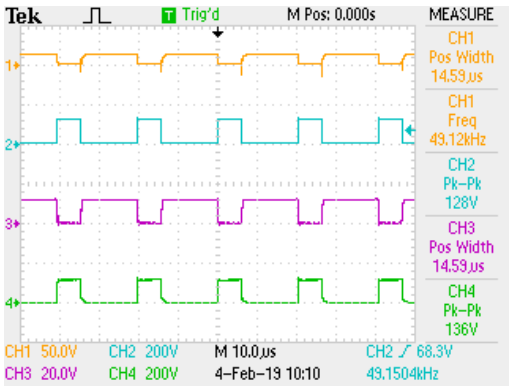

Fig. 15 Gate pulse to S_1 (V_{G1}), voltage across S_1 (V_{s1}), gate pulse to S_2 (V_{G2}), voltage across S_2 (V_{s2})

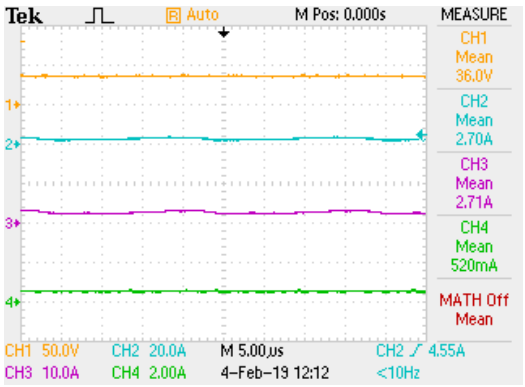

Fig. 16 Input voltage (V_{in1}), input current of Converter 1 (I_{in1}), input current of Converter 2 (I_{in2}), output current (I_0)

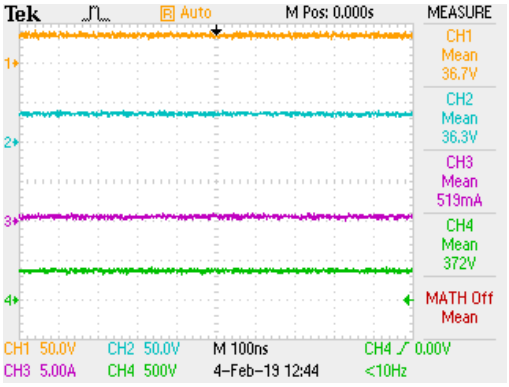

Fig. 17 Input Voltage of Source 1 (V_{in1}), Input Voltage of Source 2 (V_{in2}), Output Current (I_0), Output Voltage (V_0)

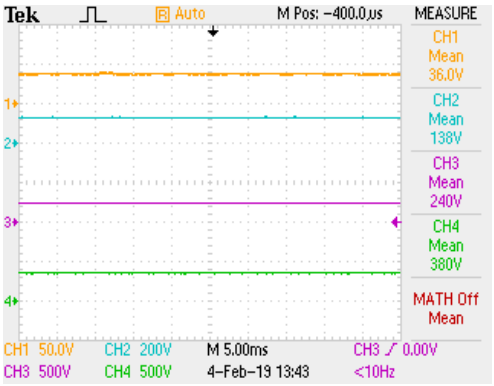

Fig. 18 Input voltage of source 1 (V_{in1}), voltage across capacitor C_1 (V_{C1}), voltage across capacitor C_3 (V_{C3}), output voltage (V_0)

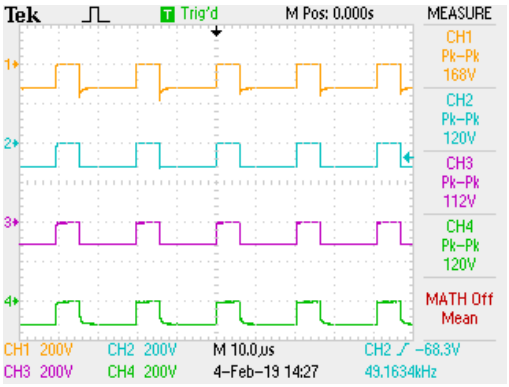

Fig. 19 Voltage across diodes from DM_1, DM_5, DM_3, DM_7 (V_{DM1}, V_{DM5}, V_{DM3}, V_{DM7})

The current drawn by the primary windings of coupled inductors follows the gate pulse switching. The switches operate in complementary manner. When the switch S_1 is ON, S_2 is OFF and vice versa. As observed from Fig. 22, the voltage across the switches is only a fraction of V_0 and matches with the design value.

When an input of $18V$ is applied from both the sources, the output voltage of each converter is $380V$ and output current is $272mA$ in Fig. 23. ORing diodes are used for parallel operation of converters 1 and 2 in topology 2.

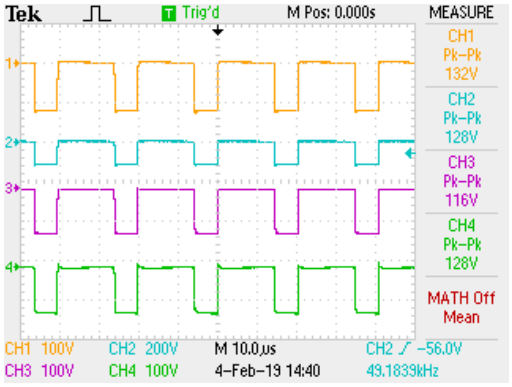

Fig. 20 Voltage across diodes from DM_2, DM_6, DM_4, DM_8 (V_{DM2}, V_{DM6}, V_{DM4}, V_{DM8})

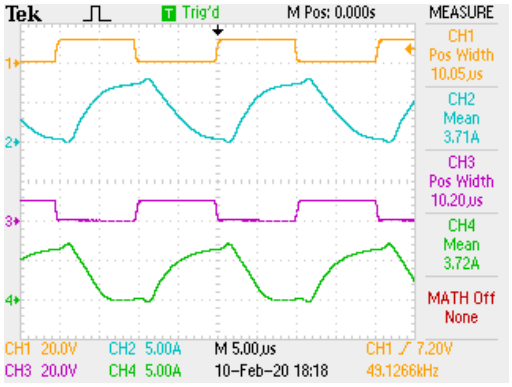

Fig. 21 Gate pulse applied to S_1 and S_2 respectively (V_{GS1}-CH1, V_{GS2}-CH3), input current through primary winding of CIs 1 and 2 respectively (I_{LP1}-CH2 , I_{LP2}-CH4)

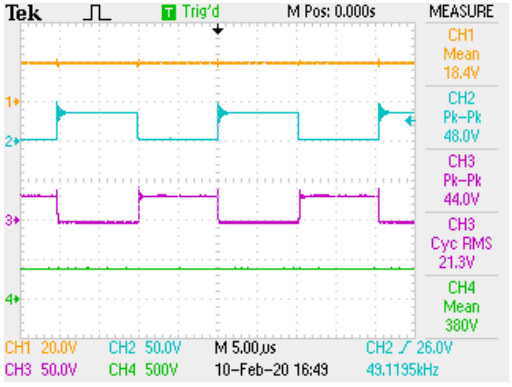

Fig. 22 Input voltage (V_{in1}), voltage across switch 1 (V_{S1}), voltage across switch 2 (V_{S2}), output voltage (V_0)

These diodes allow current flow only in forward direction and prevents supply from drawing short circuit currents. The practical power output is nearly $200W$ and the load is equally shared by both the converters.

The output voltage from voltage lift and VMC cell is collected across C_{01}. Diode capacitor modules are connected across secondary windings of Coupled inductors and these outputs are connected across C_{02} and C_{03}. The cumulative output of C_{01}, C_{02} and C_{03} gives the output voltage. These voltages are shown in Fig. 24.

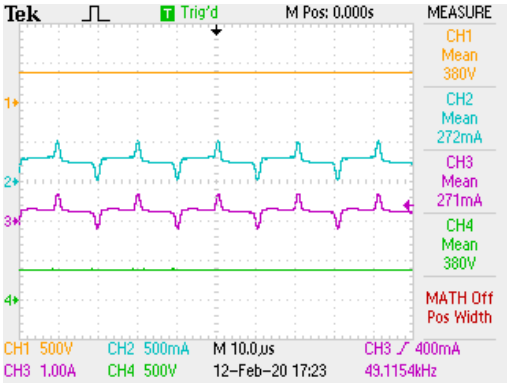

Fig. 23 Output voltage of converter 1 (V_{01}), output current of converter 1 (I_{01}), output current of converter 2 (I_{02}), output voltage of converter 2 (V_{02})

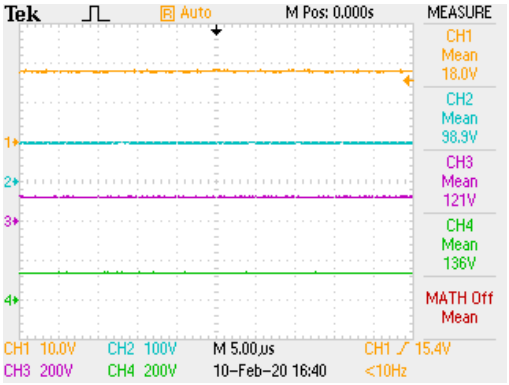

Fig. 24 Input Voltage (V_{in1}), voltage across output capacitors C_{01}, C_{02}, C_{03} (V_{C01}, V_{C02}, V_{C03})

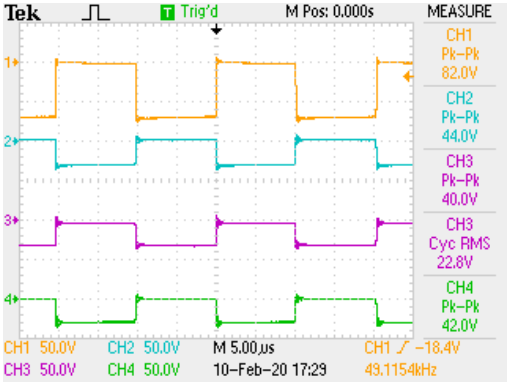

Fig. 25 Voltage across lift diode (V_{DLift}), voltage across VMC diode (V_{DM1}), voltage across VMC diode (V_{DM2}), voltage across output diode (V_{D0})

The voltage across lift diode, multiplier diodes and output diode are shown in Fig. 25. When S_1 is ON, energy is stored in L_{P1}. As S_2 is OFF, stored energy in L_{P2} is transferred to C_{1L} through voltage lift diode D_{1L} and S_1. Now C_{1L} starts charging. Since D_{1L} is forward biased, multiplier diode D_{M1} in the VMC network is reverse biased. Diodes D_{M1} and D_{M2} are complementary. Therefore D_{M2} is forward biased thereby transferring the stored energy from C_1 to capacitor C_2. The output diode D_{01} is reverse biased. The voltage stress across these diodes vary between 10% to 20% of V_0.

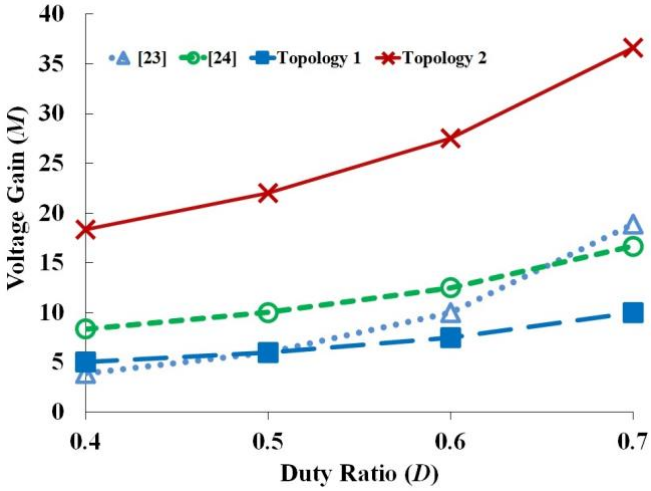

Fig. 26 Voltage gain comparison plot.

6. Comparison of Attributes of Proposed Converters

In order to appreciate the desirable features of the proposed topologies, some of the main attributes of the proposed topologies are quantitatively compared with a couple of MICs presented in literature and summarised in Table 4. The following sub-sections highlight some of the salient and desirable features of topologies 1 and 2.

6.1. Voltage Gain

The voltage gain of the converter presented in [23] varies from 3.2 to 4.75. Since, the converter presented in [23] employs discrete inductors, the additional flexibility of adjusting the turns ratio value available while using CIs is absent. The converter described in [24] uses 1 CI with a turns ratio of n=4. Hence, its voltage gain value ranges from 9.52 to 11.11. Topology 1 provides a voltage gain of 10.33 while topology 2 has higher voltage gain value of 21.11. Fig. 26 shows the voltage gain comparison plot of both topologies. In topology 1, VMC's alone contribute for gain factor. In topology 2, besides an interleaved boost with voltage lift, VMC and DCM contribute for the voltage gain.

6.2. Voltage stress on the switches

The voltage stress of the switches in [23] is about 53% of V_0 and is the highest among the converters compared. The converter presented in [23] uses 2 simple discrete inductors and yields the lowest voltage gain. Resultantly, the switches are subjected to high voltage stress levels. The converter described in [24] uses 1 CI with a turns ratio of n=4. Therefore, its switches are subjected to voltage stress value which is about one-fifth (21% precisely) of the output voltage. In both the proposed topologies, the switches are placed before the gain extension cells. Therefore, they experience low voltage stress. In topology 1, the switches are operated at D=0.716 and the stress across them is 33.33% of V_0. The voltage stress across switches in topology 2 is just 9.47% of output voltage. Topology 2 employs CIs for extending the voltage gain and yields the highest voltage gain value of 21.11. Further, the switches are also located

very close to the output while gain extension happens stage by stage. Consequently, the switches in topology 1 are subjected to the least voltage stress levels.

6.3. Voltage stress on the diodes

Diodes are located at various positions in both the proposed topologies. In topology 1, the minimum stress is 33.33% and maximum is 100% of output voltage. Similarly, the stress varies from 9.47% to 23.82% of output voltage in topology 2. The stress across diodes in topology 2 is low when compared to topology 1. The main reason for the low voltage stress is the stage by stage voltage gain extension. Further, the location of diodes in the gain extension mechanisms also plays an important role in reducing the voltage stress on the diodes. The diodes used for fabricating the converters presented in [23] experience voltage stress levels ranging from 53% to 132% of V_0. As mentioned earlier, the location of the diodes and the gain extension mechanism adopted results in high voltage stress on the diodes. The diodes of the converter presented in [24] are subjected to reasonably reduced voltage stress levels ranging from 1.5% to 84% of the output voltage.

6.4. Ratio of voltage gain(M) to total component count(TCC)

For the converter in [23], the *M/TCC* value is 0.4. Despite using only 8 components, due to the low voltage gain value, the *M/TCC* value is low and only about 0.4. The converter discussed in [24] uses 17 components. However, since the voltage gain value is double that of the converter in [23], its *M/TCC* value is the highest and works out to 0.56. The total number of components used in topology 1 and 2 are 26 and 42 respectively. The component count is the highest and second highest in both the topologies. Nevertheless, since they offer high voltage gain values, their *M/TCC* values are also reasonable. İn fact, since topology 2 offers excellent voltage gain value 21.11), despite using 42 components, its *M/TCC* value is the second highest at 0.5.

6.5. Comparison of loss distribution profile of proposed converters

The loss across the components used in proposed high gain multi-input converters are calculated using equations (3-5).

$$P_{loss-in-switches} = P_{loss-conduction} + P_{loss-switching} = I_{sw-RMS}^2 \times R_{sw-ON} + P_{sw-ON} + P_{sw-OFF} \quad (3)$$

where $P_{loss\text{-}in\text{-}switches}$ is both conduction and switching power loss in switches.

$$P_{loss-diode} = V_{d-ON} \times I_{d-AVG} + \frac{V_{d-OFF} \times I_{rr}}{2} \quad (4)$$

where $P_{loss\text{-}diode}$ is power loss in diodes.

$$P_{loss-inductor} = I_{Lpy}^2 \times R_{Lpy} + I_{Lps}^2 \times R_{Lps} + P_{iron} \quad (5)$$

Table 4. Attribute comparison of Topologies 1 and 2

	High Gain MIC's presented in			
	[23]	[24]	Topology 1	Topology 2
Input voltage (V_{in})	20V, 30V	36V, 42V	36V	18V
Output voltage (V_o)	95V	400V	372V	380V
Output Power (P_o)	60W	200W	193W	200W
Voltage gain (M)	3.2 to 4.75	9.52 to 11.11	10.33	21.11
Duty ratio (D)	0.6, 0.5	0.5	0.716	0.5
Magnetic components	2	1 CI, n =4	2	4 CI's
Total component count (TCC)	8	17	26	42
Voltage stress on the switch V_{sw} (% of V_0)	53	21	33.33	9.47
Voltage stress on the diodes V_{diode} as % of V_0 (min, max, average)	53, 132, 92.5	1.5, 84, 40.5	33.33, 100, 46.66	9.47, 35.8, 23.82
M/TCC ratio	0.4	0.56	0.4	0.5

where $P_{loss\text{-}inductor}$ is power loss in inductors.

The values of $V_{D\text{-}ON}$, $R_{SW\text{-}ON}$, I_{rr} are obtained from manufacturers datasheet. Fig. 27 shows the loss distribution profile of MICs-1 and 2 respectively.

In topology 1, 26 components are used since only two VMC gain extension cells are used. The component count in topology 2 is increased to 42 because there are gain extension cells connected to secondary of CI's. Therefore, the loss in diodes increased in topology 2 compared to topology 1. The efficiency of topology 1 is 93.43% and topology 2 is 94.14% which are nearer values.

7. Conclusion

In this paper, two non-isolated high gain multi-input converters were presented and compared. The MICs delivered 200W power to the load from two sources at

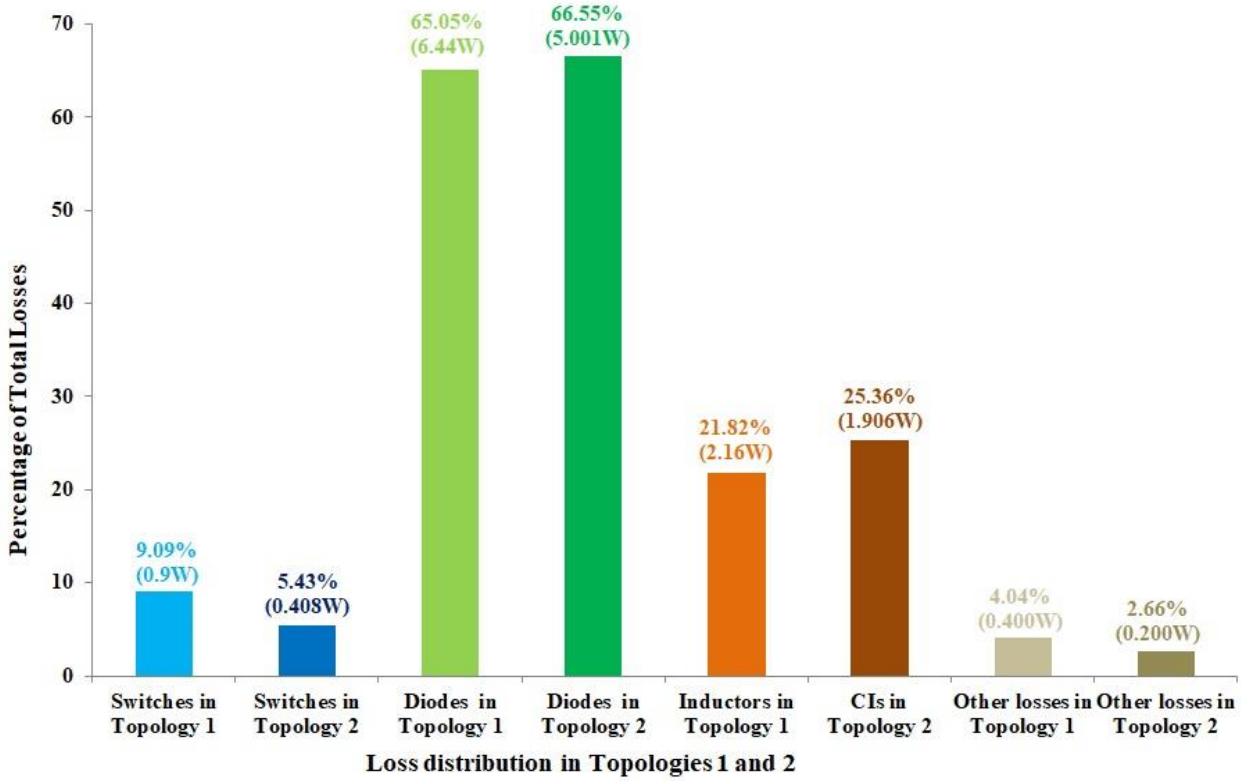

Fig. 27 Loss distribution profile of proposed topologies 1 and 2.

voltage gain values of 10.33 and 21.11. Despite operating at high voltage gain values, the stress on the devices was only a fraction (less than one-third) of the output voltage. Each of the MICs employed ORing diodes to connect two high gain DC-DC converters in parallel. Experiments were performed on both the MICs to validate the proposed voltage gain and power sharing concepts. Since ORing diodes were employed, the power demanded by the load was equally shared by the individual HG converters when both the sources were available. Based on the experiments conducted with only one source, the power delivering capability of the active converter which delivered the required power to the load was verified. The two MICs were compared to determine their suitability for renewable energy application. Considering the comparative indices, MIC-2 is preferred for integrating any two renewable energy inputs to a common DC bus.

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