Soft Switching Bridgeless Rectifier for NEV Battery Charger

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Abstract- The high efficiency soft switching bridgeless PFC rectifier with Continuous Conduction Mode (CCM) is proposed for Neighbourhood Electric Vehicle (NEV). For each switching period, the proposed converter operates both in Pulse Width Modulation (PWM) mode and resonant mode and hence termed as Hybrid Resonant PWM. Reduced Electromagnetic Interference (EMI), switching losses and voltage stress across semiconductor devices are realized in this converter by implementing the soft-switching technique. Externally Resettable Integrator (ERI) Control technique is employed in which the duty ratio control of the switch is achieved in a single switching period. This technique also rejects input voltage perturbations in one switching cycle and follows the control reference instantaneously. A 125W converter prototype is designed and simulated using PSIM software and the results are realized with experimental results. The hardware results infer that the input power factor is closer to unity and output voltage is regulated to 110V with an efficiency of 94%.

Keywords Zero Voltage Switching, Power Factor Correction, Hybrid Resonant PWM, Soft switching, Resettable Integrator Control.

1. Introduction

With the growth of technology in past years, the constant urge of efficient environment-friendly systems have been the core aim of recent inventions. Awareness about pollution and depletion of resources has resulted in the usage of EVs. Hybrid vehicles are one of the earlier proposed models of EVs. It uses more than two power sources such as Internal Combustion Engine (ICEs) to drive an electric generator which in turn powers electric motor. Pure electric vehicles that use only electricity as a power source are termed as Battery Electric Vehicles (BEVs). Another type of hybrid electric vehicle is Plug-in Hybrid Electric Vehicle (PHEV) where battery can be recharged by externally plugging in the electric power source, as well as by onboard engine and generator. Most PHEVs are preferred for passenger cars. Implementation of AC-DC charger with Power Factor Correction (PFC) [1] is essential to achieve the regulatory need of input current harmonics and output voltage regulation.

Unlike the conventional boost PFC converter, there is no diode bridge rectifier in the dual boost converter topology [4]. Thus, the count of semiconductor devices reduces in this topology. However, a dual boost converter faces many drawbacks despite of the above-mentioned advantage. Floating output with respect to ground produces Common-Mode (CM) noise which is a major drawback of the converter. Implementing input-output isolation, high startup inrush current, and switching losses poses as a major snag of the converter. Semi-bridgeless PFC converter [11] comprises two slow diodes D3 and D4 as shown in Fig 1 to reduce CM noise. Continuous conduction mode operation of the converter for high power application [13] is almost made impossible because of the reverse- recovery problem created in the MOSFET intrinsic body diode used in totem- pole converter [12]. To overcome the reverse recovery losses of the body diode in MOSFET, alternate topologies [14, 15] are proposed. But the conglomerative topology challenges its implementation. To reduce the switching losses and to truncate the problem

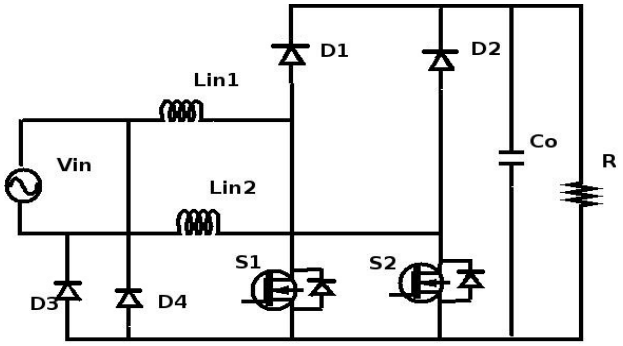


Fig. 1. Semi bridgeless AC-DC converter.

related to high-frequency operation in the above-mentioned converter many soft switching techniques [5]-[9] and topologies are suggested

Major problems faced while implementation of boost converter, dual boost converters, or/ and any soft switching boost converters are high inrush current and lack of surge protection. SEPIC and Cuk converters [16-17] control the inrush current and provides input-output isolation. But the implementation of low power applications with Cuk and SEPIC converters becomes a challenge. The converter topology [18] shown in Fig. 2 does not have high inrush current and also equipped with input-output isolation capability along with the bridgeless application. The major pitfall of the converter is that the voltage drops across the PWM switches during the high-power operation of the converter [19]. A hybrid PWM has been suggested for totem-pole bridgeless [21] converter in which the input current distortion across zero crossings is mitigated. As PWM MOSFET's are placed in series, switching losses are higher but limited to low power applications and Zero Voltage Switching (ZVS) becomes impossible in this case. Switching losses increases as the converter are operated at high switching frequency. This results in reduced efficiency of the converter and increased stress across the components.

To overcome the above drawbacks, a new High-Resolution Pulse Width Modulation (HRPWM) ZVS AC-DC PFC converter is introduced for NEV and PHEV battery charging applications. The topology overcomes the problems such as low power operation, switching losses, conduction losses, and high inrush current. The proposed AC-DC converter the input voltage is rectified and boosted. This proposed converter reduces the number of components used when opted for an AC-DC converter followed by a DC-DC converter [22-27]. The high frequency operation of the converter brings down the size of the components used. The reduced number of components consecutively brings down the cost of the converter. The reverse recovery losses in the switches are curtailed by introducing the resonant operation. The converter aims in achieving ZVS operation across the switches.

2. Proposed converter and its working principle

The proposed HRPWM converter is a bridgeless soft switching AC-DC rectifier topology with boosting action. During high frequency operation, LC tank is used in the converter to achieve resonance which ultimately obtains high gain without introducing a transformer. The soft switching technique is achieved by ZVS which reduces the switching losses and increases the efficiency of the converter.

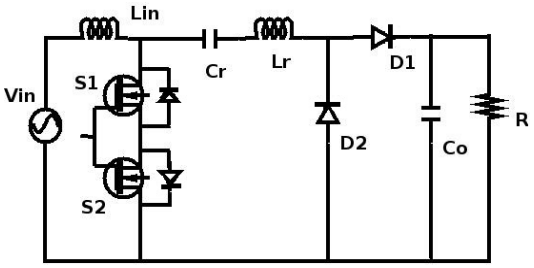


Fig 2. Bridgeless AC-DC converter

The proposed converter depicted in Fig.3 uses three MOSFET's and four diodes, (two diodes on the input side and two diodes on the output side). Two switches M1 & M2 present at the same leg of the converter is triggered with the same duty cycle. The switch M3 in the other leg is fired with duty cycle complementary to M1 and M2 along with dead-band delay. The boost inductor L1 contributes to the boost operation of the converter. The capacitor Ca, inductor La and MOSFET M3 constitute the resonance circuit. M1 and M3 undergo ZVS turn ON which reduces voltage stress across the switch and switching losses. The output diode D4 and D3 are turned OFF with di/dt and consequently decrease the reverse recovery losses of the diodes.

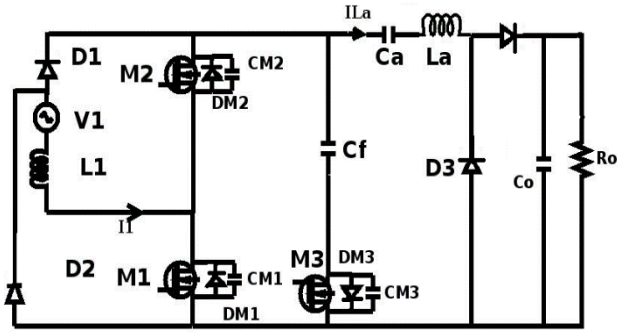


Fig. 3. The HRPWM bridgeless rectifier

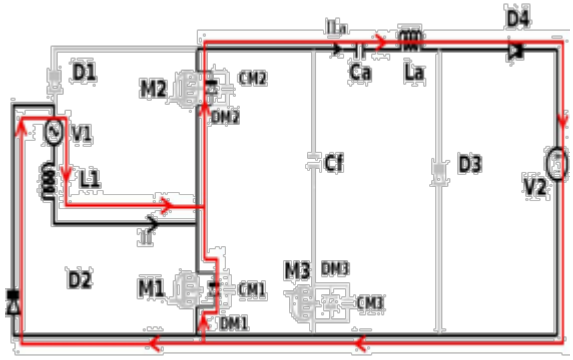
The modes of operation discussed over one switching cycle for the positive half cycle. The same operating principle can be analyzed for the negative half cycle. There are seven interval of operation and their theoretical waveforms are illustrated in Fig 5.

2.1.Interval-1(t0-t1) :

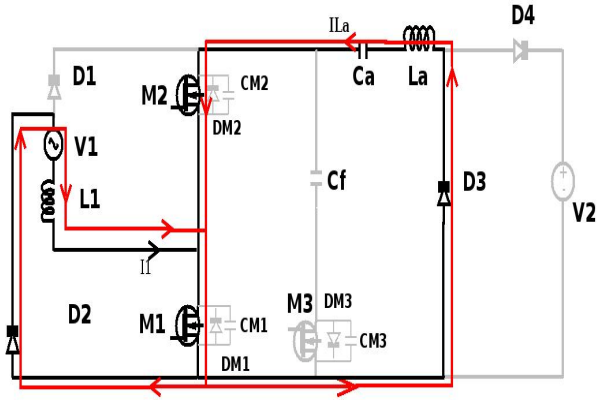
The parasitic capacitor CM3 of switch M3 is fully charged and the parasitic capacitor of M1 is fully discharged. The body diode of switch M1, clamps the current through the switch to instate ZVS in switch M1 as shown in Fig.4(a). Current through the inductor L1 and resonant inductor La is given by equation (1) and (2).

$$i_1(t) = \frac{V_1}{L_1}(t - t0) + i_1(t0) \quad (1)$$

$$i_{La}(t) = \frac{V_{Ca(min)} - V_o}{L_a}(t - t0) + i_{La}(t0) \quad (2)$$



(a) Interval 1



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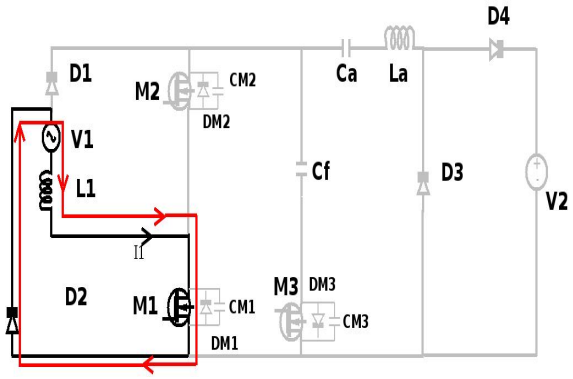
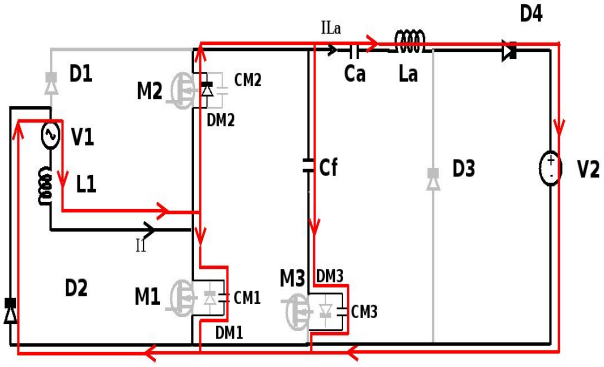
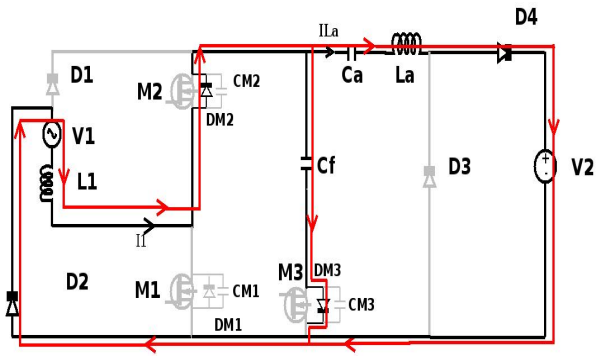


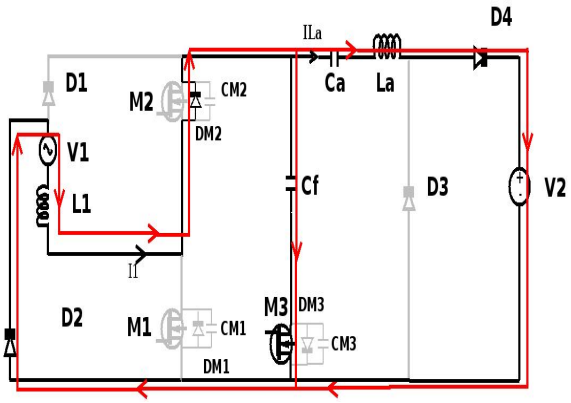
(c) Interval 3



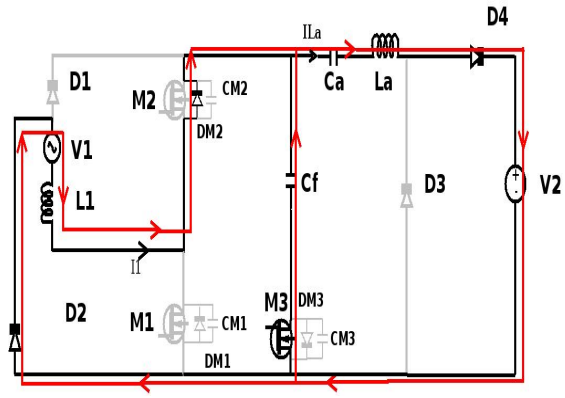
(d) Interval 4(i)



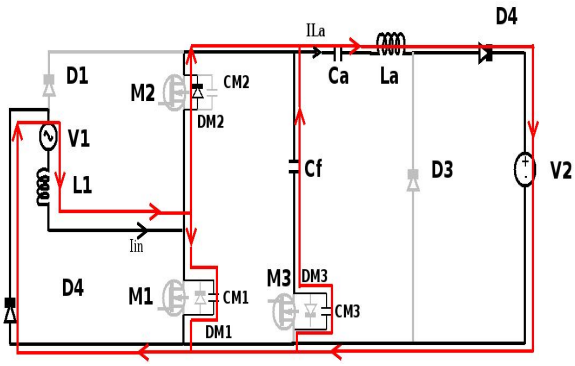
(e) Interval 4(ii)



(f) Interval 5



(g) Interval 6



(h) Interval 7

Fig.4 Modes of operation

2.2.Interval-2(t1-t2):

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{Cr(min)}}{Z} \sin(\omega_r(t-t1)) \quad (3)$$

The sum of resonant branch Ila and the input current I1 contributes to the current through the switch M1. The switch current im1 follows the resonant current Ia. The input inductor L1 stores energy through input current I1.Zero Current Switching (ZCS) is initiated by turning off diode D3 when the resonant current Ila in resonant inductor La becomes zero. Equations in (3) and (4) show the current through resonant inductor and voltage across the resonant capacitor.

$$V_{Cr}(t) = V_{Cr\,(min)}[\cos(\omega_r(t-t1)) - 1] + V_{Cr}(t1) \quad (4)$$

Where, $Z = \sqrt{\frac{L_r}{C_r}}$ and $\omega_r = \frac{1}{\sqrt{L_r C_r}}$

2.3. Interval-3(t2-t3):

Diode D3 stops conducting as the current through the resonant branch reaches zero. The boost operation occurs when the inductor L1 stores energy. This interval ends when M1 switches OFF.

2.4. Interval-4(t3-t4):

Switch M1 is turned OFF at $t = t3$. The parasitic capacitor CM1 of switch M1 is charged by input current I1 while the parasitic capacitor CM3 discharges. The body diode DM3 of M3 clamps the switch current as depicted in Fig 4(e). The expressions for input current, current through the resonant inductor and voltage across the resonant capacitor are shown in equations (5), (6) and (7).

$$i_{in}(t) = \frac{V_{in} - V_{Ca}}{L_{in}}(t - t3) + i_{in}(t3) \quad (5)$$

$$i_{Lr}(t) = -i_{Cr}(t) = \frac{V_{Cr(max)}}{Z} \sin(\omega_r(t-t3)) \quad (6)$$

$$V_{Cr}(t) = V_{Cr\,(max)}[\cos(\omega_r(t-t_3)) - 1] + V_{Cr}(t3) \quad (7)$$

Where, $Z = \sqrt{\frac{L_r}{C_r}}$ and $\omega_r = 1/(L_r C_r)$

2.5. Interval -5(t4-t5):

This interval enables ZVS turn- ON of switch M3.

2.6. Interval 6(t5-t6) :

Current through switch M3 flowing from drain to source and resonant current Ila becoming equal to input current I1 marks the beginning of this interval. Hence a change in direction of current flow across switch M3 can be observed. The turn OFF of switch M3 marks the ending of this interval.

2.7. Interval 7(t6-t7) :

The capacitor Cf is charged and body capacitor CM1 is discharged by input current I1. The body diode DM1 of switch M1 clamps the current through the switch.

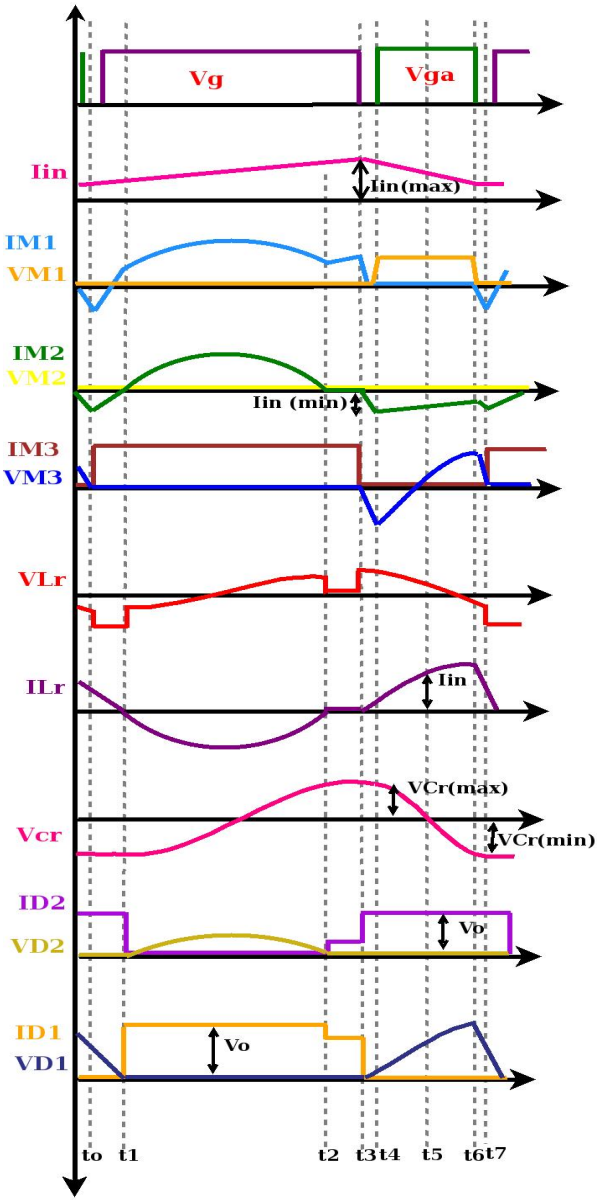


Fig 5. Theoretical waveform

3. Features of the proposed converter

- The conduction losses and heat management complexity are reduced due to the unavailability of the diode bridge rectifier.
- Switching losses are reduced, as all MOSFET's are turned ON with ZVS.
- The reverse recovery losses are minimized by turning off output diodes D3 and D4 with controlled di/dt.
- Reverse recovery losses of MOSFET body diode is eliminated by introducing resonant operation
- The proposed AC-DC converter operates with ERI control technique to achieve PFC.
- This converter, unlike totem pole converter operates in CCM which increases converter efficiency.
- The voltage across the MOSFET is almost equivalent to the output voltage of the converter.

4. Externally Resettable Integrator (ERI) controller

The externally resettable integrator is the key element in this nonlinear Control technique. The control reference is exactly equal to the average of chopped waveform in each cycle which gradually controls the duty cycle of RIC technique This unified control technique provides the ease to change control and reference inputs which prove to be suitable for both leading-edge and trailing edge modulated topologies. Fig 6 shows the implementation of ERI [20] for the proposed converter. The error voltage amplifier is given the output voltage which is sensed by a voltage sensor where the error voltage is amplified.

Externally resettable integrator, integrate the amplified error signal from error voltage amplifier and produce a variable slope ramp voltage in a switching cycle. The voltage reference generated by the combination of error voltage and inductor current is compared with the varying slope ramp voltage. The integrator is reset and the switch is turned OFF when the integrator ramp voltage and the voltage reference are equal. At the end of each switching cycle, the integrator circuit is reset and the ramp restarts again from zero for consecutive switching cycle**.** During input perturbation, the ramp voltage reaches the inductor current, the fault is suppressed in one switching cycle and the switch turns OFF. The dynamic output voltage is integrated. A change in output voltage immediately affects the slope of the integrated output voltage.

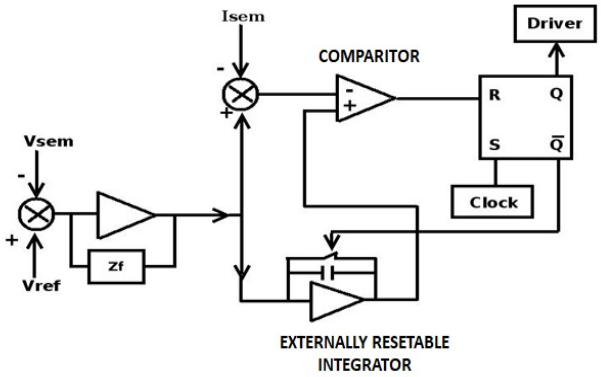


Fig.6. RIC technique

The integration of the output voltage is constant in each cycle because of the power source which affects the duty ratio d. The power source perturbation should not be sensed by the average value of output voltage as it follows the control reference as predicted. With switching function $k(t)$ and frequency $f_s=1/T_s$, the switch operates efficiently,

$$k(t) = \begin{cases} 1 & 0 < t < TON \\ 0 & TON < t < TS \end{cases} \quad (8)$$

TON is the duration for which the switch is ON for each cycle. TOFF is the duration at which the switch remains OFF for each cycle. $TON + TOFF = TS$ where TS is the total time interval.

The duty ratio $d = T_{ON}/T_S$ is modulated by analog control signal. $V_{ref}(t)$.$x(t)$ is the chopped input signal. The switch function $k(t)$ and the pulse width and frequency of the output switch are the same, while envelop of y(t) is $x(t)$.

$$y(t) = k(t).x(t) \quad (9)$$

If the frequency bandwidth of either input signal $x(t)$ or control signal $V_{ref}(t)$ is much lower than that of the switching frequency fs, then the effective output switch signal is

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)\,dt = x(t).V_{ref}(t) \quad (10)$$

The product of input signal $x(t)$ and control signal $V_{ref}(t)$ forms the output signal $y(t)$. This makes the switch operate nonlinearly. The average value of the control signal in each cycle and the average value of chopped waveform at switch output are equal.

$$\frac{1}{T_s}\int_0^{T_{ON}} x(t)\,dt = \frac{1}{T_s}\int_0^{T_S} V_{ref}(t)dt \quad (11)$$

Therefore the output signal is instantaneously controlled within one cycle.

$$y(t) = \frac{1}{T_s}\int_0^{T_{ON}} x(t)dt = \frac{1}{T_s}\int_0^{T_S} V_{ref}(t)dt = V_{ref}(t) \quad (12)$$

This type of control is called ERI control. The output of the switch is given by

$$y(t) = V_{ref}(t) \quad (13)$$

The input signal disturbances are fully rejected and the control signal is linearly passed entirely through the switch.

5. Design Specifications

The AC-DC boost converter is designed and implemented for 125W. The ERI technique is used to achieve the PFC of this proposed soft switching bridgeless rectifier. The duty cycle is calculated from the conversion ratio from equation (14).

$$\frac{V_2}{V_1} = \frac{1}{1-D} \quad (14)$$

Where V_2 is output voltage in Volts, D is Duty cycle and V_1 is input voltage in Volts. The voltage stress across the power switches and diodes almost equal the output voltage V_2. The maximum stress across M1 and M2 is expressed in the equation below.

$$V_{M\_max} = V_2 + V_{Ca(max)} \quad (15)$$

During steady-state operation of the converter, the load current and average current across D3 and D4 are equal. Thus average load current is obtained from interval 2 & 4 is

$$I_{D_3(avg)} = \frac{V_2}{R_o} = \left[\frac{1}{T_a}\int_0^{\frac{T_a}{2}} V_{Ca(max)}\sqrt{\frac{C_a}{L_a}}\sin(\omega_a t).dt\right] \quad (16)$$

Where R0 is the load resistance in ohms, Ta is the total time period in seconds. The maximum voltage across the resonant capacitor ($V_{Ca(max)}$) is

$$V_{Ca(max)} = \frac{I_2}{2C_a f_s} \quad (17)$$

Where, Ca is the resonant capacitor in µF, is the resonant inductor in µH, the switching frequency in kHz, I2 is the output current in A. The design of resonant capacitors is given as

$$C_a = \frac{I_2}{2V_{Ca(max)} f_s} \quad (18)$$

The di/dt found in the datasheet of diode D4 is chosen to design the inductor La. The current ramp rate is determined by external circuit, thus La is determined by

$$L_a = \frac{V_2}{di/dt} \quad (19)$$

The design of boost inductor ($L1$) and capacitor (Cf) is expressed as

$$L1 = \frac{V_1 D}{f_s \Delta I_L} \quad (20)$$

$$Cf = \frac{V_2 D}{\Delta V_C R_0} \quad (21)$$

5.1. ZVS condition:

Switch M1 should be turned ON during interval (t0 –t1) to achieve ZVS. When the switch M1 is not turned ON in this interval, CM1 recharges. Hence the time delay between the ON time of M1 and turn OFF period of M3 is critical to achieve ZVS operation. The optimum period to achieve ZVS operation is one-quarter of the resonant period formed by La and Ca.

$$t_{delay} = \frac{\pi\sqrt{L_a C_{M1}}}{2} \quad (22)$$

To completely discharge capacitor CM1 there should be sufficient energy storage in resonant inductor La, along with the time requirement constraint. For ZVS turn - ON of switches M1 & M2 in condition (23) must be satisfied to achieve soft switching.

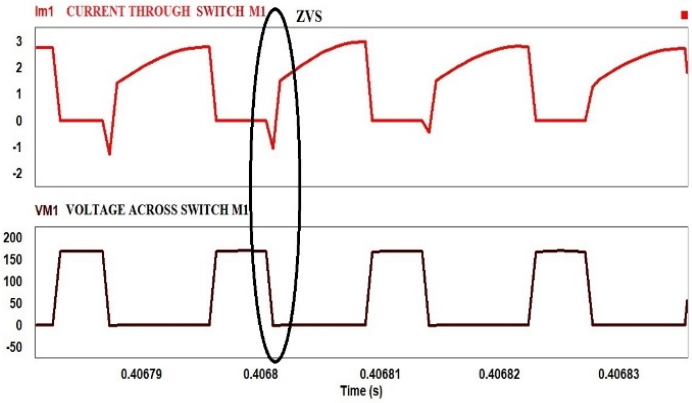
$$\frac{1}{2} L_a \left(I_{La(peak)} - I_{La(min)}\right)^2 > \frac{1}{2} (C_{M1} + C_{M2}) \left(\frac{V_1}{1-D}\right)^2 \quad (23)$$

At interval t3 when PWM switches are turned OFF, ZVS in auxiliary switch M3 is achieved. To completely discharge the capacitor CM3, there should also be required energy stored in inductor L1. Hence condition for ZVS turn ON of switch M3 is

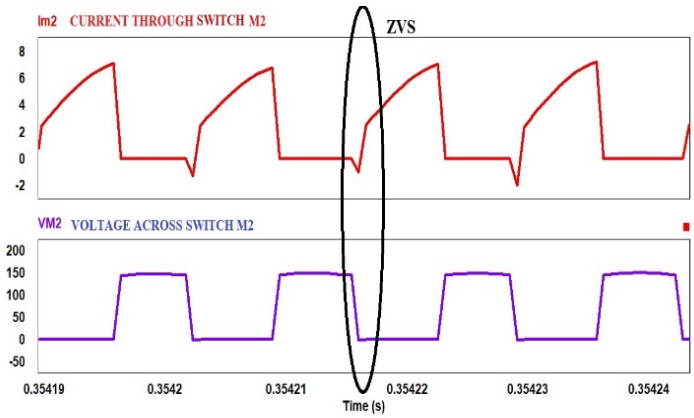
$$\frac{1}{2} L_{in} I_{in(max)}^2 > \frac{1}{2} (C_{s1} + C_{sa}) \left(\frac{V_{in}}{1-D}\right)^2 \quad (24)$$

6. Simulation Results

The converter is simulated with the design parameters listed below in Table1. The simulation is done using PSIM software. The pulses with the duty cycle of 70% is given to switch M1, M2, and 20% duty cycle with appropriate dead time to M3. ERI control improves the input power factor from 0.7 to 0.97. The current through the boost inductor L1 is sinusoidal. The ZVS operation of switches M1, M2 and M3 are achieved by resonant inductor La and capacitor Ca as shown in Fig 7(a),(b), and (c) respectively. The voltage across the MOSFET and current through the switch M1 is analyzed in Fig 7(a) for ZVS operation. Similarly, the current through M2 & M3 and voltage across M2 & M3 are analyzed for ZVS operation. ZCS operation achieved by diode D3 is shown in Fig 7(d).



(a)



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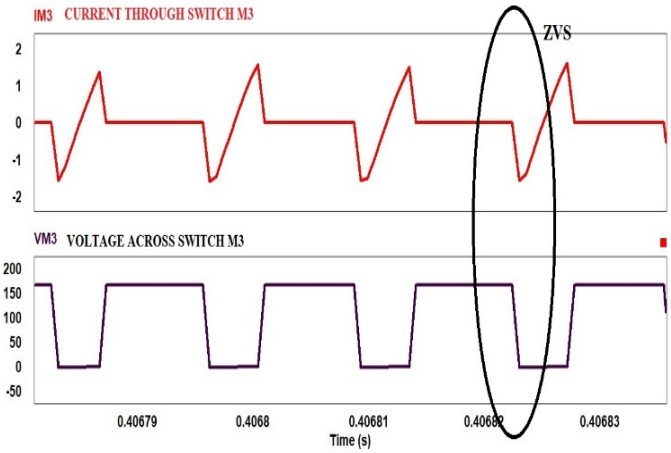
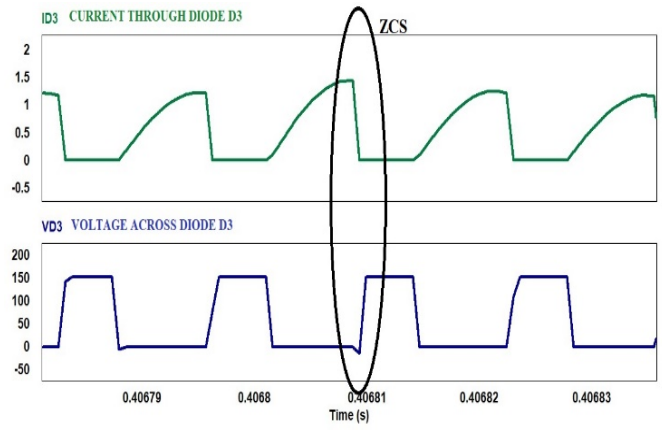


(c)



(d)

Fig.7. (a) ZVS operation of switch M1 (b) ZVS operation of switch M2 (c) ZVS operation of switch M3 (d) ZCS operation of diode D3.

Table 1. Design parameters

PARAMETERS	RATINGS
Output Power(P_o)	125W
Voltage Input(V_1)	50V
Voltage Output(V_2)	125V
Switching Frequency(f_s)	70kHz
Inductor(L_1)	3mH
Resonant Inductor (L_a)	20µH
Resonant Capacitor (C_a)	1µF
Output Capacitor (C_o)	470µF,400V

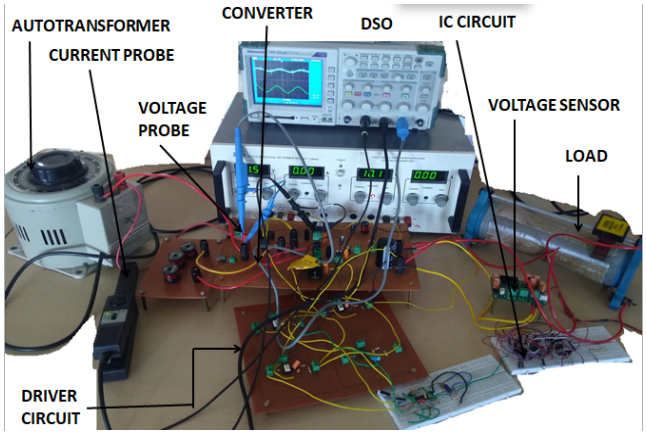


Fig.8. Experimental set up of the converter

7. Hardware Specifications

The hardware prototype is designed and tested for 125W as shown in Fig 8. Fig 9(a) shows the gating pulses with switching frequency of 70kHz given to M1, M2 and M3. The switches M1 and M2 are triggered with 70% duty cycle, while switch M3 is triggered using a delay circuit. Fig 9(b) depicts the voltage of 47.2(peak to peak) across the input diode. The hardware components with specification, ratings and requirements are shown below in Table 2.

The closed loop hardware is implemented using IC IR1150 (RIC technique) with the delay circuit. IR1150 is used for fixed frequency ac-dc converter to improve the power factor at the input end and regulate the output voltage at the load end. The shunt voltage sensor senses the output voltage which is given to the RIC IC. The external clock of the controller IC is synchronized with the switching frequency of the main switches.

The voltage across resonance capacitor (Ca) is portrayed in Fig 10(a). The ZVS operation of M1, M2, M3 are comprehended in Fig 10 (b), (c) and (d) respectively. The waveforms clearly depict the resonance state of the main switches. The output waveform of 125W with output voltage of 112V (mean value) and the output current of 1.11A (mean value) is perceived in Fig 10(e). The converter was also tested for 170W.

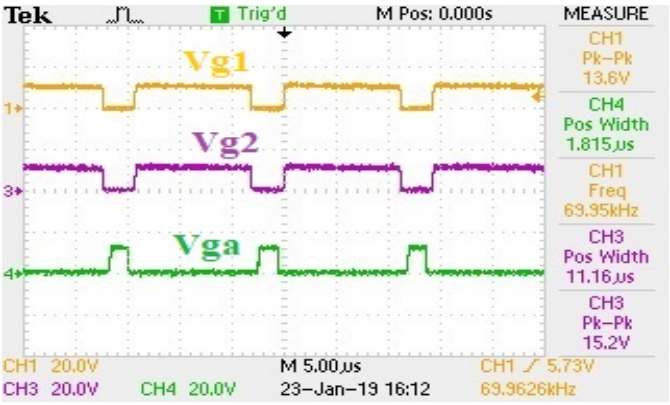


Fig.9.(a). Gating pulses to MOSFET switches

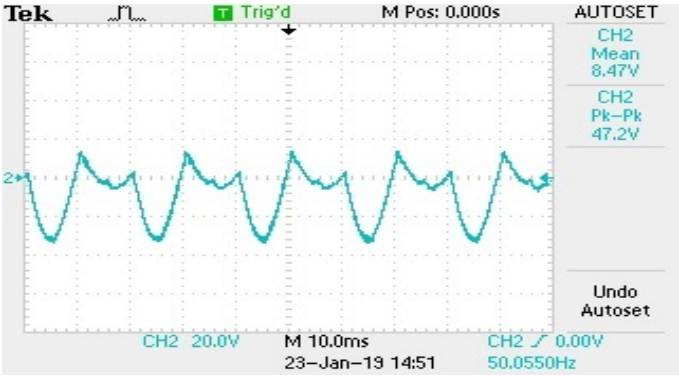


Fig.9.(b). Input diode voltage

The waveform at the input side is power factor corrected. For the input voltage of 52.4V and 110V output is obtained on the load side. This is shown in Fig 10(f). Power factor of 0.981 is realized in closed loop hardware with power of 102 W. The graph also infers the shape of input current is sinusoidal and in phase with the supply voltage. The introduction of resonance circuit with soft switching improves the converter's efficiency. In Fig. 11 (a) it is shown that the efficiency of the converter increases with increase in load.

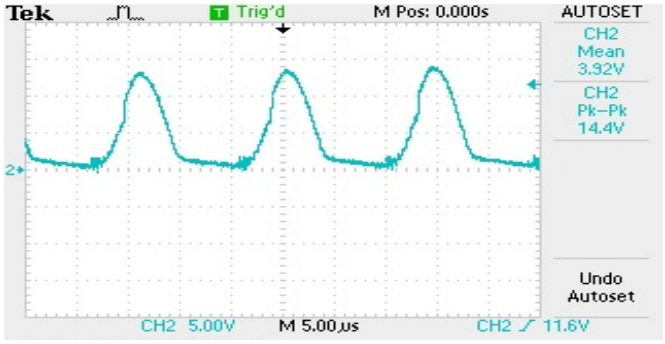


Fig.10.(a). Voltage across capacitor Ca

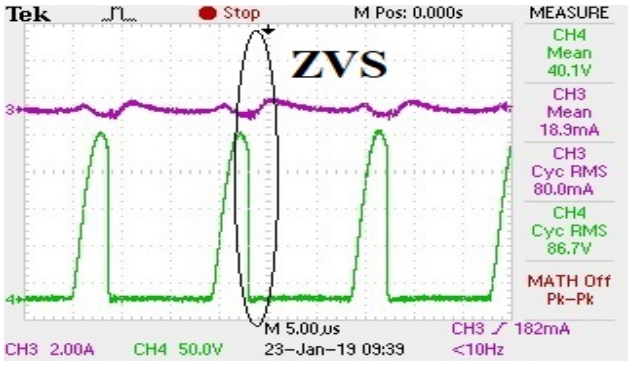


Fig.10.(b). ZVS of switch M1

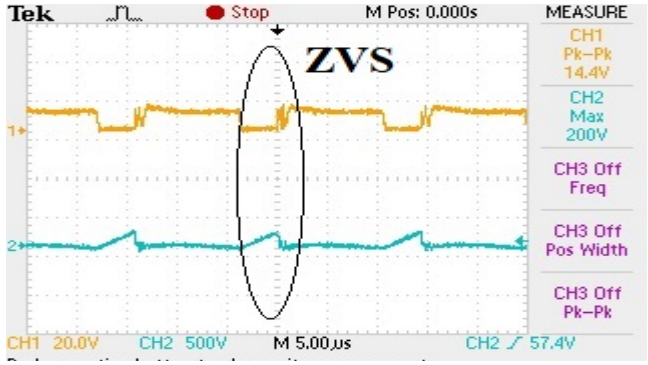


Fig.10.(c). ZVS of switch M2

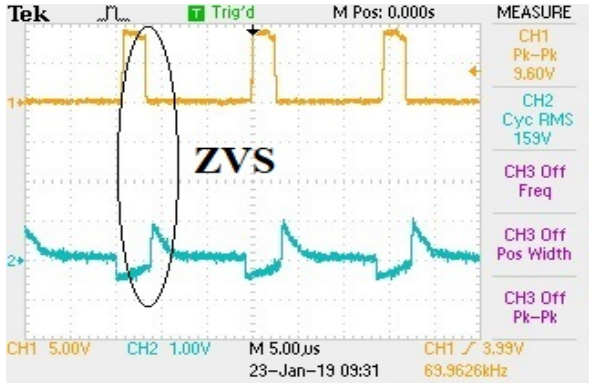


Fig.10.(d). ZVS of switch M3

Table 1. Converter components

Name of the component	Part Number	Ratings
N- Channel MOSFET	IRF840	500V, 8A
Diode	RHRP8120	1200V, 8A
Boost Inductor	PVC-2-10502L(Ferrite Core)	3mH,15A
Resonant Inductor	PVC-2-223-05L(Ferrite Core)	22µH, 25A
Resonant Capacitor	Electrolytic	1µF,250V
Output Capacitor	Electrolytic	450µF,400V

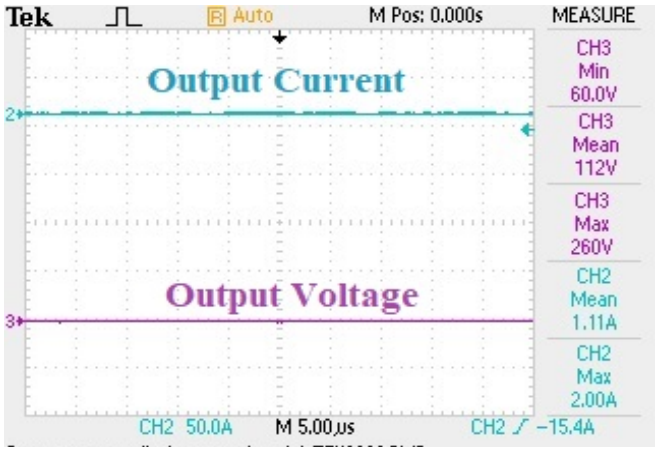


Fig.10.(e). Output waveforms for 125W

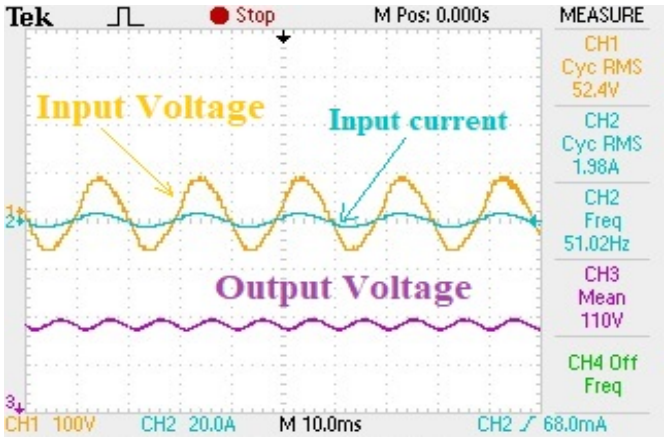
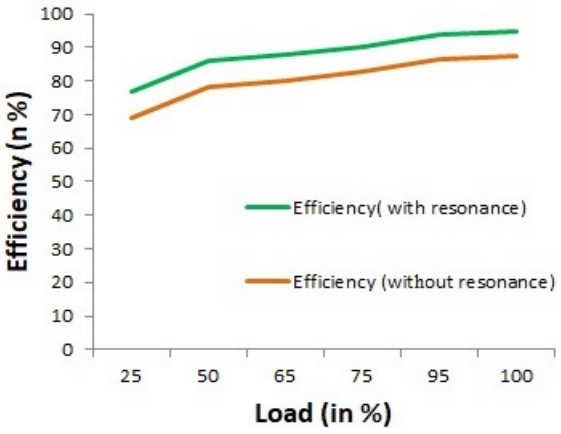
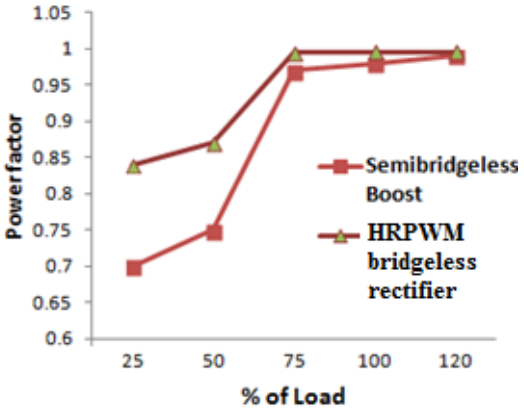


Fig.10.(f). Input and output waveforms of HRPWM bridgeless converter



(a)



(b)

Fig 11.(a) Efficiency Vs Load curve (b) Power factor Vs Load(%).

It is also realized that the same converter with hard switching operates with lesser efficiency (<70% at light load and 84% at full load condition). At resonance condition, the efficiency of the converter is increased to 94%. The power factor variation of the proposed converter with regard to load is displayed in Fig 11(b). The power factor variation is compared with the semi-bridgeless PFC boost converter and the graph infers that at light load condition (25%) the HRPWM converter achieves a power factor of 0.84 whereas the semi-bridgeless topology attains a power factor of 0.7. At full load condition, both the converter achieves power factor closes to unity.

8. Conclusion

The front-end soft switching bridgeless boost AC-DC converter is proposed for NEV application. With the implementation of soft switching techniques, the switching losses in the proposed converter are reduced. It is realized that the HRPWM converter with soft switching technique proves to be more efficient than the conventional converter. The theoretical waveforms and the modes of operation of converter with design parameters are thoroughly analyzed. The implementation of closed-loop control of the converter with RIC technique reduces the input perturbation and quickly follows the control reference.

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